Techniques for the Design of a Low Noise, High Dynamic Range, High Gain, Wideband Amplifier for Analogue OEIC Applications

A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

Shuchin Taher

M.Eng

School of Electrical and Computer Engineering

College of Science Engineering and Health

RMIT University

May 2014

Declaration

I certify that except where due acknowledgement has been made, the work is that of the author alone; the work has not been submitted previously, in whole or in part, to qualify for any other academic award; the content of the thesis/project is the result of work which has been carried out since the official commencement date of the approved research program; any editorial work, paid or unpaid, carried out by a third party is acknowledged; and, ethics procedures and guidelines have been followed.

Shuchin Taher

May 2014

Table of Contents

LIST OF FIGURES..... 6

LIST OF TABLES..... 11

DECLARATION..... 13

ACKNOWLEDGMENTS..... 14

PUBLICATIONS..... 15

DEDICATION..... 16

1 CHAPTER ONE: INTRODUCTION..... 17

1.1 OVERVIEW AND BACKGROUND..... 18

1.2 MOTIVATION AND LITERATURE REVIEW..... 19

1.3 AIMS AND OBJECTIVES..... 22

1.3.1 Objective 1: Investigation and Comparison of Transistor, Semiconductor and Photodetector Technologies 23

1.3.2 Objective 2: Comparison of Amplifier Topologies..... 25

1.3.3 Objective 3: Circuit Design Techniques for SFDR Improvement.. 25

1.3.4 Objective 4: Transistor Design Options..... 25

1.4 THESIS ORGANIZATION..... 26

2 CHAPTER TWO: INITIAL CONSIDERATIONS..... 28

2.1 INTRODUCTION..... 28

2.2 EXAMPLES OF CURRENT REALIZATIONS..... 29

2.2.1 Example 1: AlGaAs/GaAs PIN/FET Photoreceiver..... 30

2.2.2 Example 2: GaAs MSM/FET Photoreceiver..... 31

2.2.3 Example 3: AlGaAs/GaAs PIN/HBT Photoreceiver..... 32

2.2.4 Example 4: SiGe/Si PIN/HBT Photoreceiver.....33

2.2.5 Example 5: InAlAs/InGaAs PIN/HEMT Photoreceiver on GaAs substrate..... 34

2.2.6 Example 6: InAlAs/InGaAs WPD/HEMT Photoreceiver on InP substrate..... 36

2.2.7 Example 7: InGaAs/InP PIN/HBT Photoreceiver..... 37

2.2.8 Hybrid assembly..... 38

2.3 COMPARISION AND SELECTION OF PHOTODETECTOR TECHNOLOGY 39

2.4 COMPARISION AND SELECTION OF TRANSISTOR TECHNOLOGY 41

2.4.1 HEMT (High Electron Mobility Transistor) 42

2.4.1.1 Technical difference from regular homojunction FETs 42

2.4.1.2 Fabrication procedure..... 44

2.4.1.3 Operating principle 45

2.4.2 HBT (Heterojunction Bipolar Transistor)..... 45

2.4.2.1 Technical difference from regular BJTs..... 46

2.4.2.2 Fabrication procedure..... 46

2.4.2.3 Operating principle 48

2.4.3 Comparison of HEMT and HBT in Light of the Objectives of this Work 51

2.4.3.1 Arguments in favour of Selecting HEMT Technology for this Work 51

2.4.3.2 Arguments in favour of Selecting HBT Technology for this Work 51
2.4.4 Final Selection of Transistor Technology and Justification 52
2.5 SELECTION OF SEMICONDUCTOR MATERIALS 53
2.5.1 Comparison of Transistor Semiconductor Technologies 54
2.5.1.1 Arguments in favour of using Si with SiGe in this work 54
2.5.1.2 Arguments in favour of using GaAs with AlGaAs in this work 54
2.5.1.3 Arguments in favour of using InP with InGaAs in this work 55
2.5.2 Final Selection of Transistor Semiconductor Technology (Materials) and Justification 56
2.6 CONCLUSION 57
3 CHAPTER THREE: COMPARISON OF AMPLIFIER TOPOLOGIES..... 58
3.1 INTRODUCTION..... 58
3.2 CIRCUIT TOPOLOGIES..... 59
3.2.1 Shunt-series Transimpedance Amplifier..... 60
3.2.2 Feedback Transimpedance Amplifier with Common-Base Input Stage..... 61
3.2.3 Distributed Amplifier Employing Negative Resistance..... 61
3.3 COMPARISION METHODOLOGY..... 63
3.3.1 Transistor Simulation Setup 63
3.3.2 Calibration against Measured Results 67
3.3.2.1 DC Calibration 67
3.3.2.2 AC Calibration 69

3.3.3 Other Considerations 70
3.4 RESULTS..... 70
3.5 SUMMARY OF FINDINGS AND CONCLUSION..... 74

4 CHAPTER FOUR: CIRCUIT DESIGN TECHNIQUES FOR SFDR IMPROVEMENT..... 76
4.1 INTRODUCTION..... 76
4.2 REFERENCE DESIGN..... 77
4.3 SFDR ENHANCEMENT TECHNIQUES WITH DESIGN EXAMPLES 80
4.3.1 Technique 1: Replacement of Emitter follower Section..... 80
4.3.2 Technique 2: Adjustment of Amplifier Load..... 86
4.3.3 Technique 3: Adjustment of Cascode Base Capacitor..... 92
4.4 RESULTS AND OBSERVATIONS..... 95
4.5 STABILITY CONSIDERATIONS 98
4.6 CONCLUSION..... 99

5. CHAPTER FIVE: TRANSISTOR DESIGN OPTIONS..... 100
5.1 INTRODUCTION..... 100
5.2 REFERENCE DEVICE DESIGN..... 103
5.3 DEVICE SIMULATION METHODOLOGY..... 104
5.3.1. Mobility models 106
5.3.1.1. Caughey and Thomas mobility model 106
5.3.1.2. Parallel Electric Field-Dependent Mobility model 106
5.3.2. Recombination models 106
5.3.2.1. Concentration dependant Shockley-Read-Hall model 106

5.3.2.2. Auger recombination model 106

5.3.3. Carrier Statistics models 107

5.3.3.1. Bandgap Narrowing model 107

5.3.3.2. Fermi-Dirac statistics model 107

5.3.4. Impact ionization model 108

5.4 VALIDATION AGAINST MEASURED RESULTS..... 108

5.5 INFLUENCE OF COLLECTOR DOPING REDUCTION..... 109

5.6 INFLUENCE OF SPACER DOPING AND THICKNESS VARIATION 113

5.6.1 Spacer Doping Variation..... 113

5.6.2 Spacer Thickness Variation..... 116

5.7 EMITTER WIDTH AND BASE THICKNESS VARIATION 121

5.7.1 Emitter Width Variation..... 121

5.7.2 Base Thickness Variation 121

5.8 RESULTS AND DISCUSSION..... 124

5.9 VALIDITY OF FINDINGS IN ABSENSE OF MEASURED RESULTS....128

5.10 RECOMMENDATIONS BASED ON RESULTS..... 129

5.11 CONCLUSION..... 130

6. CHAPTER SIX: CONCLUSION AND FURTHER WORK..... 132

6.1 CONCLUSIONS..... 132

6.2 FURTHER WORK..... 135

REFERENCES..... 137

List of Figures

Figure 1.1: A typical optical fibre communication system comprising an optical modulator, optical fibre, photodetector and transimpedance amplifier..... 19

Figure 1.2: Co-axial cables currently used in electronic warfare applications [104]..... 21

Figure 2.1: Cross-sectional view of the PIN/FET photoreceiver of Example 1 [80]..... 30

Figure 2.2: Cross-sectional view of the PIN photoreceiver discussed in Example 2 [81] 31

Figure 2.3: Cross-sectional view of the PIN/HBT photoreceiver of Example 3 [82].... 33

Figure 2.4: Cross-sectional view of the PIN/HBT photoreceiver of Example 4 [83].... 34

Figure 2.5: Cross-sectional view of the PIN/HEMT photoreceiver of Example 5 [84].. 35

Figure 2.6: Integration scheme of the WPD/HEMT photoreceiver of Example 6 [85].. 36

Figure 2.7: Cross-sectional view of the PIN/HBT photoreceiver of Example 7 [7]..... 37

Figure 2.8: Cross-sectional view of a HEMT in Depletion-mode [87]..... 43

Figure 2.9: Energy-band diagram of a HEMT in (a) Depletion-mode (b) Enhancement-mode [87] 44

Figure 2.10: Example GaAlAs/GaAs HBT (a) epitaxial layer structure (b) Cross sectional view [87] 47

Figure 2.11: Energy-band diagram of a HBT [89] 48

Figure 3.1: Shunt-series transimpedance amplifier topology. 60

Figure 3.2: Transimpedance amplifier with common-base input stage. 61

Figure 3.3: Schematic circuit of a single stage of Cohen's HBT distributed amplifier.. 62

Figure 3.4: Large signal equivalent circuit model ADS schematic and the large signal model parameter values for the transistor referenced from [45] 64

Figure 3.5: Large-signal equivalent circuit model of the InP/InGaAs SHBT [45] 65

Figure 3.6: Large-signal equivalent circuit model of the InP/InGaAs SHBT [45] 66

Figure 3.7: (a) Measured and modelled IC-VCE characteristics under a constant IB bias condition reported in [45]. (b) IC-VCE characteristics under a constant IB bias condition produced through ADS simulation in this work 68

Figure 3.8: (a) Measured and modelled S-parameters from 0.5 GHz to 20 GHz for bias operating conditions of {IB=1.0mA, VCE=1.25V} (left) and {IB=1.8mA, VCE=1.0V} (right) as reported in [45]. (b) S-parameters from 0.5 GHz to 20 GHz for bias operating conditions of {IB=1.0mA, VCE=1.25V} (left) and {IB=1.8mA, VCE=1.0V} (right) produced through ADS simulation in this work 69

Figure 3.9: Gain characteristics of the three topologies. 72

Figure 3.10: The output power as a function of input current for the first harmonic and IM3 products of the (a) shunt-series, (b) common-base input and (c) distributed transimpedance amplifiers at 10 GHz. The noise floor is also presented (calculated for a 10 MHz noise bandwidth). 73

Figure 4.1: Schematic of a single gain stage of the Reference design by Cohen[25] 78

Figure 4.2: Transimpedance gain vs. frequency characteristics and the large signal SFDR produced by the reference design (Cohen [25]) at 30 GHz. 79

Figure 4.3: Two-tone spectral analysis on each of the four gain stages of the standard amplifier showing the effect of the emitter follower section on the linearity of the amplifier at 30(±0.05) GHz and an amplifier input current of 2.2 mA 81

Figure 4.4: Schematic of a single gain stage of the altered design with the emitter follower section replaced by a parallel RC section. 82

Figure 4.5: Two-tone spectral analysis on each of the four gain stages of the altered amplifier showing the effect of the replacement of the emitter follower section with

the parallel RC section on the linearity of the amplifier at 30(±0.05) GHz and an amplifier input current of 2.2 mA 84

Figure 4.6: Results for Technique 1 design example: (a) Changed Transimpedance gain vs. frequency characteristics (b) Large signal SFDR produced by the Technique 1 design example at 10 GHz (c) Large signal SFDR produced by the Technique 1 design example at 20 GHz (d) Large signal SFDR produced by the Technique 1 design example at 30 GHz 85

Figure 4.7: Third order IMD contours generated from load-pull simulation of a single gain stage of the reference design, at 30 GHz and at an input power level of -25 dBm. $Z_{L,4}$ values for Z_0 = 50 Ω and Z_0 = 23.19 Ω are shown. The contour step size is 1 dB ... 88

Figure 4.8: Schematic design of the tapered line transformer network used for wideband impedance matching of the amplifier Z0 of 23.19 Ω to a 50 Ω load across the bandwidth of the amplifier, i.e. 30 Ghz 90

Figure 4.9: Results for Technique 2 design example: (a) Changed Transimpedance gain vs. frequency characteristics (b) Large signal SFDR produced by the Technique 2 design example at 10 GHz (c) Large signal SFDR produced by the Technique 2 design example at 20 GHz (d) Large signal SFDR produced by the Technique 2 design example at 30 GHz 91

Figure 4.10: Third order IMD contours generated from load-pull simulation of the common emitter HBT transistor X2 (in Figure 4.1). Load impedances of X2 for C1 values ranging from 10 pF to 0.25 pF in steps of -0.05 pF are shown. The contour step size is 1 dB. 93

Figure 4.11: Results for Technique 3 design example: (a) Changed Transimpedance gain vs. frequency characteristics (b) Large signal SFDR produced by the Technique 3 design example at 10 GHz (c) Large signal SFDR produced by the Technique 3

design example at 20 GHz (d) Large signal SFDR produced by the Technique 3 design example at 30 GHz 94

Figure 5.1: Structure of the Reference SHBT showing (a) All layers and (b) Meshing. 105

Figure 5.2: (a) Simulated and Measured I-V characteristics curves of the reference SHBT from [67]. (b) I-V characteristics curves of the reference SHBT acquired through Device Simulation in this work. 108

Figure 5.3: Results for four different collector doping profiles. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V). 110

Figure 5.3 (continued): Results for four different collector doping profiles (at V_{be}=0.95V and V_{ce}=0.95V). (c) Current gain in dB versus frequency. (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). 111

Figure 5.4: Results for four different spacer doping profiles. (a) Base Collector Capacitance Cbc versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V). 114

Figure 5.4 (continued): Results for four different spacer doping profiles. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). 115

Figure 5.5: Results for four different spacer thicknesses. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V). 117

Figure 5.5 (continued): Results for four different spacer thicknesses. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). 118

Figure 5.6: Results for three different emitter widths. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V). 119

Figure 5.6 (continued): Results for three different emitter widths. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). 120

Figure 5.7: Results for three different base thicknesses. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V). 122

Figure 5.7 (continued): Results for three different base thicknesses. (c) Current gain in dB versus frequency (at V_{be}=0.95V and Vce=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). 123

List of Tables

Table 2.1: Summary of Advantages and Disadvantages of various types of Photodiodes 41

Table 2.2: Summary of Advantages and Disadvantages of selecting each of the HEMT and the HBT for this work 52

Table 2.3: Bandgap energy and applicable spectral range for various materials used in the construction of photodetectors [93]. 56

Table 2.4: Comparison of AlGaAs/GaAs HBT, Si/SiGe HBT and InGaAs/InP HBT for different FOMs [34]. 57

Table 3.1: Simulated Transimpedance Amplifier Performance at 10 GHz (Noise Bandwidth = 10 MHz). 71

Table 4.1: SFDR and Transimpedance Gain Comparison between the Reference Design and designs altered using the three Techniques. 96

Table 4.2: SFDR Transimpedance Gain Comparison between different Combinations of Techniques. 97

Table 5.1: SHBT Epilayer Structure. 104

Table 5.2: Summary of the Influence of Collector Doping Concentration on the Linearity, Bandwidth and Gain of InP HBTs. 125

Table 5.3: Summary of the Influence of Spacer Doping Concentration on the Linearity, Bandwidth and Gain of InP HBTs..... 125

Table 5.4: Summary of the Influence of Spacer Layer Thickness on the Linearity, Bandwidth and Gain of InP HBTs. 126

Table 5.5: Summary of the Influence of Emitter Width on the Linearity, Bandwidth and Gain of InP HBTs. 127

Table 5.6: Summary of the Influence of Base Thickness on the Linearity, Bandwidth and Gain of InP HBTs. 128

Table 5.7: Summary of recommended modifications to device specifications. 130

Declaration

I certify that except where due acknowledgement has been made, the work is that of the author alone; the work has not been submitted previously, in whole or in part, to qualify for any other academic award; the content of the thesis is the result of work which has been carried out since the official commencement date of the approved research program; any editorial work, paid or unpaid, carried out by a third party is acknowledged; and, ethics procedures and guidelines have been followed.

Shuchin Taher

9th January 2015

Acknowledgements

I would like to acknowledge and express my sincerest gratitude for the helpful and supportive guidance of my supervisor, Associate Professor James R. Scott throughout the duration of this project. His knowledge and resolve guided me through the many challenges of the project and helped me to improvise when needed. In addition, I appreciated the help and cooperation of my second supervisor, Associate Professor Anthony Holland.

I would also like to thank the School of Electrical and Computer Engineering at RMIT University for supporting this research through the SECE Scholarship. Additionally, my sincerest thanks go towards the technical and administrative staff at the School of Electrical and Computer Engineering for their support on various matters.

I thank my friend and fellow researcher Soumitra Niyogi for his support and friendship during the project, and my friend and colleague Kusha Panta for his enthusiastic encouragement during the final days of the project and his relentless efforts and encouragement to keep me on track through the writing of the thesis.

Finally, I would like to thank my wife and both of my parents for their understanding, endless patience and constant encouragement during my studies.

Publications

S. Taher and J. Scott, "A comparison of InP HBT transimpedance amplifier topologies for high dynamic range photonic links," in *Proceedings of Asia-Pacific Microwave Conference*, 2009.

S. Taher and J. Scott, "An investigation of tradeoff options for the improvement of spurious-free dynamic range in HBT transimpedance distributed amplifiers," *Progress In Electromagnetics Research Letters*, Vol. 30, 67-79, 2012.

This thesis is dedicated to my loving wife,

Rapti

Chapter One:

Introduction

1.1 OVERVIEW AND BACKGROUND

Photo receiver circuits are a major component in fibre optic transmission systems. In today's fibre optic communication systems, photoreceivers play an important role and contribute significantly to the overall performance of the communication system. These photoreceivers, also sometimes referred to as optoelectronic receivers or optoelectronic integrated circuit (OEIC) receivers are most efficiently realized by monolithic integration of compatible photodetectors and transimpedance amplifier circuits. The design of such OEIC photoreceivers has in recent years attracted a lot of

interest from researchers around the world [1-13]. While much of the work done on OEIC photoreceivers in the past were on Gallium Arsenide (GaAs) based chips, researchers more recently have recognized Indium Phosphide (InP) as an attractive compound semiconductor for microwave-photonic applications, and certain advantages that it has over GaAs when it comes to designing high performance OEICs, such as much higher speed and compatibility with fibre optic systems operating at wavelengths that inherently feature low loss and low dispersion of light energy [6]. As a result many researchers have switched to InP as their semiconductor of choice for designing OEIC receivers, especially since the 1990's. However, a review of the literature shows that most of the work done in the development of OEIC receivers are aimed at enhancing commercial data communication systems and are therefore designed to work with low power digital signals of as high bandwidth i.e. data rates as possible [1-7, 105]. While the motivation behind striving to improve commercial digital communication standards is understandable, there are certain potential applications of OEIC receivers (elaborated further in Section 1.2) with a different set of performance criteria, such as the photoreceiver's ability to handle analogue signals over a very wide dynamic power range in addition to low noise and high bandwidth capabilities. A thorough and up-to-date literature review on OEIC photoreceivers reveals that despite ample improvements made to traditionally desirable attributes of photoreceivers, such as bandwidth, data rate, responsivity, etc. [10-13], very few attempts appear to have been made to improve the analogue performance, in particular the dynamic range of the photoreceivers. The reason for this is that photoreceivers thus far are rarely used in any applications other than digital data communication systems, for which a high dynamic range is not among the list of desirables. However, as mentioned earlier, there are some applications where these

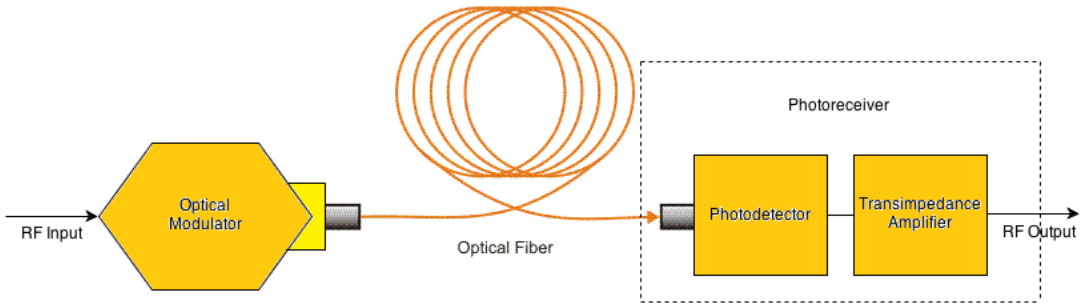


Figure 1.1: A typical optical fibre communication system comprising an optical modulator, optical fibre, photodetector and transimpedance amplifier

attributes can be very useful, and therefore this research will be attempting to develop techniques to achieve these desirables.

1.2 MOTIVATION AND LITERATURE REVIEW

As previously mentioned, there has been a considerable amount of work done on photoreceivers in the last decade, particularly OEIC implementations on InP, where the photodetector and transimpedance amplifier are integrated together on the one chip [7, 12, 25]. Photoreceivers with up to 100 V/W optoelectronic gain at 46.5 GHz optoelectronic bandwidth have been realized using InP HBTs [12]. Such photoreceivers are most commonly used in digital applications, and as such most of the work done on them has primarily focused on improving gain, bandwidth and noise performance due to their importance in such applications. Works focusing on linearity and dynamic range of OEIC photoreceivers have been scarce as these figures of merit are substantially unimportant in most commercial applications of OEIC photoreceivers. However, there are certain analogue communication applications where there is a high linearity and dynamic power range requirement. Examples of

such applications include military radar warning receivers, which currently use RF coaxial cables to transfer analogue radar information across a relatively wide dynamic power range and wide bandwidth to the central hub, as shown in Figure 1.2. There are other similar applications where RF coaxial cables are used to handle high dynamic power range wideband analogue signals within the military and even in commercial flights and flight stations where radars are used. These applications are often airborne in nature. As a result, some of the most desired features in the technology used in these applications include low weight, immunity to electromagnetic interference and a low noise performance in addition to high bandwidth and high dynamic power range performance. At the moment RF cable technology dominates these applications because it offers a relatively high dynamic range performance [76]. Optical fibre links have the potential to be an attractive replacement for the RF links used in these applications as they offer a wide range of advantages over the currently used technology, the major ones being; significant weight advantages, immensely higher bandwidth support, EMI immunity and flexibility. The primary drawback in such a replacement is the fact that a high dynamic power range of the links is a priority for these applications due to the operational nature of radar in general. On the other hand, the composite dynamic range of such optical fibre links after being modulated and preamplified, is rather limited due to the limited dynamic range of the modulator and the photoreceiver (preamplifier) [76]. The primary causes for this limitation are, the RIN noise produced at the optical modulator, the shot and thermal noise produced at the photoreceiver, and the nonlinear performance of both the modulator and the photoreceiver [76]. If this limitation can be overcome in optical modulators and the photoreceivers, the RF links used in these applications can be replaced with optical fibre links. It should be noted that, defence applications such as these require the

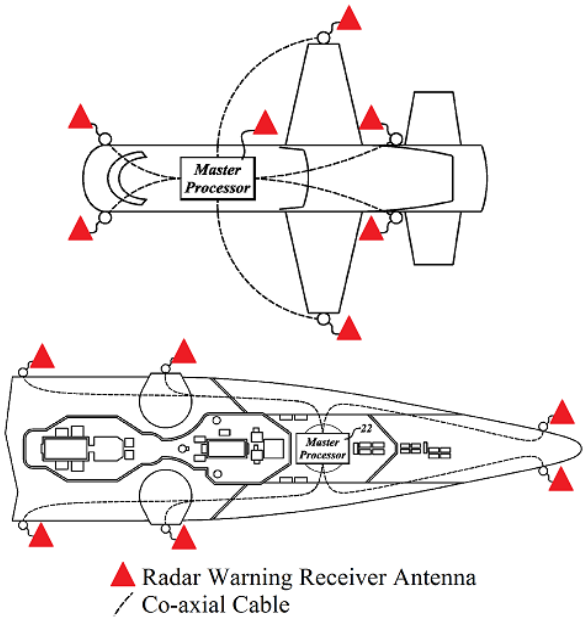


Figure 1.2: Coaxial cables currently used in electronic warfare applications [104]

system to also feature high gain and high bandwidth as well as high linearity and high dynamic range [78].

The dynamic range in analogue photonic links is currently limited primarily by the linearity of the optical modulator at the transmitter, and secondly by the OEIC receiver [76]. Optical modulators with highly improved SFDR values have recently been reported [15, 79]. Assuming that the dynamic range of modulators improves further, the optical receivers will become significant in determining the overall dynamic range of wide-band analogue photonic links. It is therefore important to work on improving the dynamic range of the receivers as well. The transimpedance amplifier generates a significant portion of the nonlinearities in a photoreceiver. There have been a number of papers in recent years focusing on improving the linearity of amplifiers by improving their output third-order intercept point (OIP3) performance [16–20], however they are mostly power amplifiers intended for wireless and radio applications rather than low noise transimpedance amplifiers suitable for analogue

optoelectronic applications. On the other hand, recent works that focused on amplifier linearity in analogue applications suitable for defence electronic systems such as radar and electronic warfare platforms, were based on HEMT technology [21, 22], which is not as compatible with OEIC devices such as PIN photodetectors as HBT technology, in terms of fabrication simplicity. There have also been some recent works that used various techniques to improve the linearity of HBT LNAs [23, 24]. However, they are not suitable for electronic warfare platforms due to their limited bandwidth performance. Hence, there is a need for amplifiers featuring high linearity and dynamic range, as well as a high gain and bandwidth for use in OEIC receivers for certain defence applications as discussed above. Understandably, because there are a number of additional design objectives (higher linearity and dynamic power range, fabrication simplicity, etc.) in this work in contrast with past works, tradeoffs will need to be made in other areas, and therefore the other desirables, i.e. bandwidth, gain, etc. will understandably be inferior to the best currently existing photoreceiver. The challenge in this work will be to develop design techniques to balance all desirables to be reasonably workable in the applications that the OEIC receiver will be intended for.

1.3 AIMS AND OBJECTIVES

A photoreceiver generally consists of a photodetector and a preamplifier, which is generally a transimpedance amplifier. This work will primarily focus on the preamplifier portion of the photoreceiver, which significantly contributes to the nonlinearities in the photoreceiver. These nonlinearities along with noise are

responsible for the dynamic power range limitation of the receiver. As already mentioned, a transimpedance amplifier is generally used as a preamplifier in OEIC receivers, because the input to the amplifier is a photocurrent generated by the photodetector. As discussed in Section 1.2, the focus of this work is primarily electronic warfare applications, and for such applications, the figures of merit of amplifiers used in photoreceivers that are most important are listed as follows:

- High Spurious-free Dynamic Range (SFDR)
- High amplifier linearity
- Low noise
- High amplifier gain
- High bandwidth
- Fabrication simplicity (Low cost)

As such, the primary focus of this work will be on these figures of merit of a transimpedance amplifier that is suitable for use in a photoreceiver. Improvement and optimization for these figures of merit of the transimpedance amplifier, especially its linearity and SFDR, is the overall goal of this work. The key objectives are elaborated in more detail as follows.

1.3.1 Objective 1: Investigation and Comparison of Transistor, Semiconductor and Photodetector Technologies

Answers to the following research questions need to be determined first.

1. Which transistor technology is most suitable to be used and goes the furthest towards meeting the goal of the research (wide bandwidth and high dynamic range)? High-electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are both promising candidates in this case and are both capable of pushing receiver bandwidths up to 50 GHz and higher [8], [9]. Each of them has their advantages that can potentially be utilized and disadvantages that can potentially end up as a trade-off. However, which has a net advantage over which once all parameters are accounted for in detail is up to the research to find out.

2. Which semiconductor technology is most suitable to be used and goes the furthest towards meeting the goal of the research? Which semiconductor material and layers should be used with the selected transistor technology in light of the goals of the project?

3. Which photodetector technology is more suitable to be integrated on a single chip with the selected transistor technology with minimum performance loss, minimum fabrication complexity and maximum results in light of the goal of the research? The primary photodetectors that are compatible with bipolar and field-effect transistors are the PIN and MSM diode structures. Like the transistor technologies, each of these has their pros and cons, which will need to be distinctly judged before a decision on which to use can be made. Notably, although this work will not focus on the photodetector, this decision is important because it will have an influence on design considerations with regards to the transistors used in the amplifier in future chapters.

1.3.2 Objective 2: Comparison of Amplifier Topologies

The next objective will be to determine the optimum circuit topology once both the photodetector and transistor structures are determined. As previously discussed, existing work has focused on wideband, low noise performance. The following research questions will be considered.

1. Are the current feedback-based circuit designs optimal for maximising dynamic range performance?

2. Are other amplifier topologies capable of providing superior performance?

In order to answer these questions, performance simulations of the existing feedback based amplifier circuit topologies will be compared with those of other known amplifier topologies in light of our amplifier figures of merit of interest. Based on a comparison of results, the amplifier circuit topology that is most suitable and goes the furthest towards meeting the goals of the project will be determined.

1.3.3 Objective 3: Circuit Design Techniques for SFDR Improvement

Once the amplifier circuit topology is selected, the next objective will be to develop techniques to improve or optimize the SFDR performance of the amplifier at the circuit design level.

1.3.4 Objective 4: Transistor Design Options

The final objective will be to develop techniques at the device design level to improve or optimize the linearity, gain and bandwidth of individual transistors within an amplifier. Such improvements at the transistor level would in turn result in the improvements of the previously mentioned figures of merit at the amplifier level,

which is the main goal of the project. The development of techniques for such improvements is the principle objective.

1.4 THESIS ORGANIZATION

This thesis is divided into six chapters, covering a thorough discussion of the research. A brief description of each chapter is given as follows.

Chapter One: Introduction

This chapter provides an overview and background on the state of the art and the potential applications of photonic links in electronic warfare applications, and advantages thereof are discussed. A brief introduction to the project is presented followed by the aims and objectives of this work.

Chapter Two: Initial Considerations

The available transistor technologies and their pros and cons in light of the goal of the project are investigated in this chapter in order to decide on the transistor technology best suited for this research, and justification of the chosen transistor technology is presented. Similarly, a semiconductor technology and photodetector technology are also selected for the project through appropriate investigation and the justifications for the decisions are discussed.

Chapter Three: Comparison of Amplifier Topologies

Three different known amplifier topologies are discussed and their linearity, gain, bandwidth, SFDR, and other performances are compared via simulations. The results

from the comparisons are analysed and the amplifier topology most suitable for this work is chosen based on these results.

Chapter Four: Circuit Design Techniques for SFDR Improvement

Three different circuit alteration techniques for improving the linearity and SFDR of the previously chosen amplifier topology are analysed and verified through simulation. It is shown that these techniques can be combined to gain further improvement in overall performance.

Chapter Five: Transistor Design Options

The influence of various geometrical and doping alterations of the transistor on desired figures of merit, i.e. gain, bandwidth, linearity, etc. are investigated in detail via TCAD device simulation, and the results are used to suggest techniques to improve performance at the transistor level.

Chapter Six: Conclusion and Further Work

A conclusion is made on the basis of the extensive work carried out. Suggestions and possibilities for the expansion of this work are discussed in the further work.

Chapter Two:

Initial Considerations

2.1 INTRODUCTION

Before the main research can commence on the photoreceiver, a few initial decisions are required to be made, such as the selection of materials, transistor types, etc. These decisions are important, as the rest of the research will be substantially shaped and influenced by them. As such each of them should be made carefully with the goal of the research in mind. As already discussed in Sections 1.2 and 1.3, and also shown in Figure 1.1, the photoreceiver is basically a photodetector followed by a

transimpedance amplifier. However, before the selection of the photodetector and transistor can commence, the semiconductor technology, i.e. semiconductor material system for the photoreceiver should be selected keeping in mind that one of our objectives is to integrate both the photodetector and the transimpedance amplifier on a single substrate. In the second part of the chapter (Section 2.2) some of the past realizations of integrated photoreceivers based on various selections that are made for the semiconductor technology, photodetector technology and transistor technology are presented and reviewed. From this section we gather a general idea about the semiconductor technologies, photodetector technologies and transistor technologies that are generally used in the field for this purpose. In the third part of this chapter (Section 2.3), we focus on the selection of the photodetector technology by firstly discussing suitable photodetector types including those used in past realizations, comparing the pros and cons of each of these photodetector types in light of our objectives and then presenting a justification for the final selection of the photodetector type that was made. In the fourth part of the chapter (Section 2.4), we focus on the usual transistor technologies, including detailed descriptions of candidate transistor technologies, followed by a presentation of their pros and cons, which were weighted and a final selection was made, the justification for which is also presented. A similar selection process for the combination of semiconductor materials is carried out in the fifth part of the chapter (section 2.5).

2.2 EXAMPLES OF CURRENT REALIZATIONS

In this section, we take a close look at existing realizations of photoreceivers where the photodetector and the transistor(s) used for the transimpedance amplifier are integrated on a single substrate. In particular our focus will be on the photodetector

and transistor types used, semiconductor materials used, chosen fabrication and device structure, and the complexity of device fabrication resulting from these choices. These observations are used as a guide to making our own choices on these matters in the project, which are discussed in following sections.

2.2.1 Example 1: AlGaAs/GaAs PIN/FET Photoreceiver

In this realization [80], a PIN photodiode was monolithically integrated with a GaAs FET transistor. AlGaAs/GaAs semiconductors were used for the PIN photodetector. MOCVD is used to first grow the multilayers for the PIN, on top of which the GaAs layers for the FET is grown. The FET layers are later etched away from the section which is used for the PIN photodetector. Although the growth is a single step process, a considerable number of layers are grown as the PIN photodetector and the FET do not share any layers, which adds to the complexity of the fabrication process. A cross sectional view of this photoreceiver is shown in Figure 2.1.

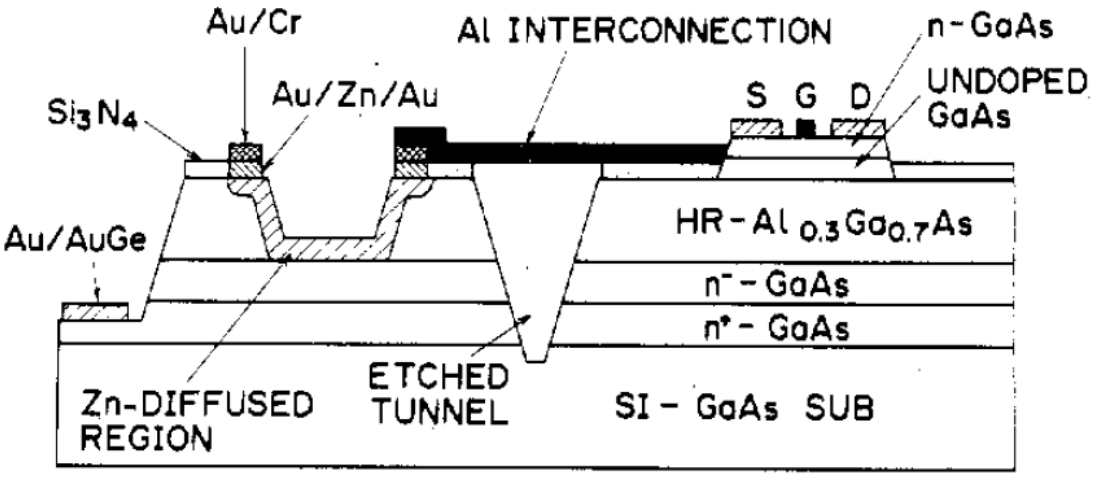


Figure 2.1: Cross-sectional view of the PIN/FET photoreceiver of Example 1 [80].

From this realization, in which a photodetector absorption layer thickness of 3.5 um and carrier concentration as low as 5e14 cm-3 was used, dark current as low as 7e-10A (the PD being biased at -5V) and a quantum efficiency of approximately 70% was achieved. These performance results were determined through examining the device using a 0.78 um optical wavelength light emitting diode.

2.2.2 Example 2: GaAs MSM/FET Photoreceiver

In this realization [81], an MSM (metal-semiconductor-metal) photodiode was monolithically integrated with a GaAs FET transistor. The single step fabrication process for this photoreceiver is very simple and straight forward as monolithic integration of the MSM diode and the FET is achieved without having to introduce any additional processes except for FET fabrication though MOCVD and formation of electrodes for the diode. A cross sectional view of this photoreceiver is shown in Figure 2.2.

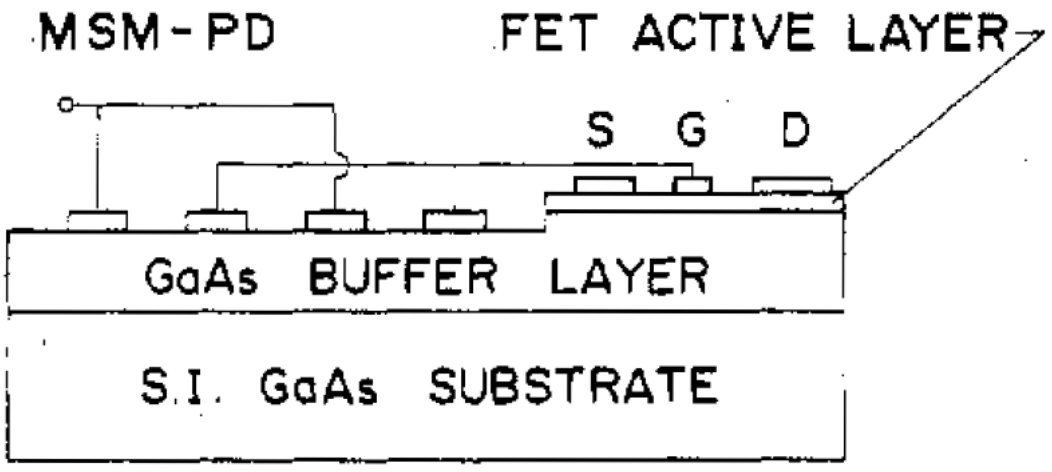


Figure 2.2: Cross-sectional view of the PIN photoreceiver discussed in Example 2 [81].

From this realization, using 3 um wide and 100 um long fingers with 3 um interspacing between the MSM electrodes, a dark current value less than 5 uA (the PD being biased at 15V) was achieved. The DC external photosensitivity was determined to be 2.2 A/V from results determined through measuring the device using a 0.83 um optical wavelength light emitting diode. From this result, the internal sensitivity was determined to be 4.4 A/V, which corresponds to an external quantum efficiency of 330%, which in turn indicates a photocurrent gain within the MSM PD.

2.2.3 Example 3: AlGaAs/GaAs PIN/HBT Photoreceiver

In this realization [82], a PIN photodiode was monolithically integrated with a AlGaAs/GaAs HBT transistor. As can be observed in Figure 2.3, in this case the same fabricated epitaxial layers are shared by both the PIN photodetector and the base and collector of the HBT. Thus the fabrication process for this photoreceiver is also a single step process where the layers for both the photodetector and the transistor are grown at the same time, which contributes significantly to the simplicity of the fabrication process, compared with the fabrication process for example 1. Notably, the

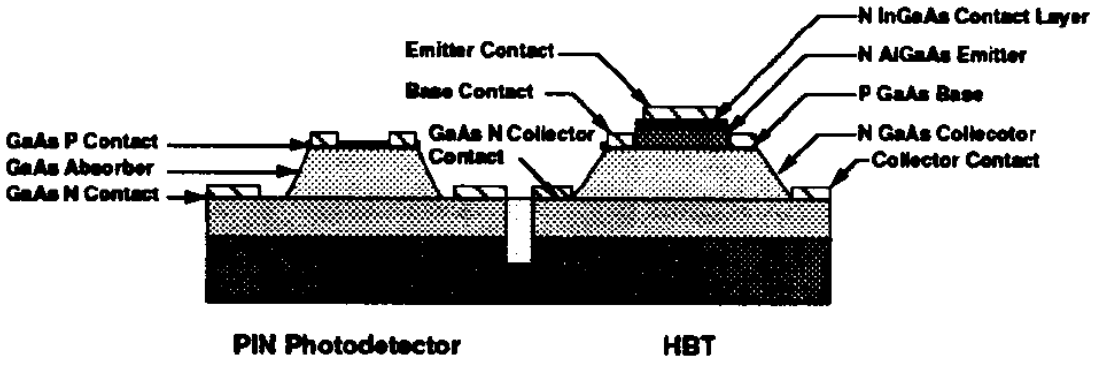


Figure 2.3: Cross-sectional view of the PIN/HBT photoreceiver of Example 3 [82].

drawback in this case is that the photodiode demands the absorption layer to be thick in order to have an excellent responsivity while the HBT requires the corresponding layer which forms the collector to be thin in order to have excellent speed and bandwidth. However, balancing this conflict to a reasonable level via appropriate tradeoffs in order to receive decent performances from both the photodetector and the HBT is generally feasible. A cross sectional view of this photoreceiver is shown in Figure 2.3.

In terms of performance, bandwidths as high as 13 GHz for optical signals in the 0.8 um was reported for this OEIC receiver. A transimpedance gain of 250Ω was also reported for the receiver. Leakage current of only 40 nA (the PD being biased at -3V) and a responsivity value of 0.244 mA/mW was achieved for the photodetector, which indicates a 35.6% quantum efficiency.

2.2.4 Example 4: SiGe/Si PIN/HBT Photoreceiver

This realization [83] is similar to example 3 in terms of fabrication scheme, in that a top illuminated PIN photodiode was monolithically integrated with a HBT transistor, where the same fabricated epitaxial layers are shared by both the PIN photodetector and the base and collector of the HBT. As such, similar advantages as example 3 were achieved in terms of fabrication simplicity. The primary difference from example 3 is that SiGe and Si layers were used in this case instead of AlGaAs and GaAs layers used in example 3. In other words, the PIN transistor and the HBT are both based on SiGe/Si semiconductor technology. A single step MBE procedure is used to grow the Si/SiGe layers for both the transistor and the photodetector at the same time. A cross sectional view of this photoreceiver is shown in Figure 2.4.

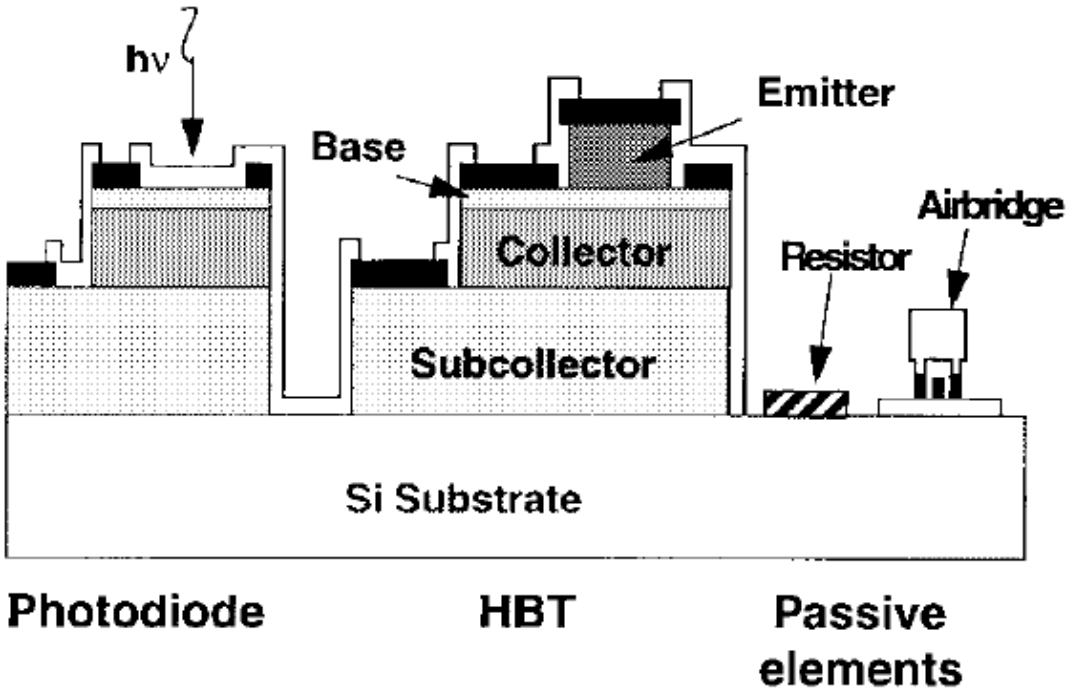


Figure 2.4: Cross-sectional view of the PIN/HBT photoreceiver of Example 4 [83].

Performance wise, although the f_T and f_{max} of the HBT was 23 GHz and 34 GHz respectively, the achieved bandwidth of the HBT was only 1.6 GHz. The optical bandwidth of the photoreceiver was also restricted by the PD to only 460 MHz. However, a transimpedance gain of 52.2 dBΩ and a responsivity of 0.3 A/W at a wavelength of 0.85 um (which corresponds to a 43% quantum efficiency) was achieved from this realization.

2.2.5 Example 5: InAlAs/InGaAs PIN/HEMT Photoreceiver on GaAs substrate

In this realization [84], a top illuminated PIN InGaAs/InAlAs photodiode was monolithically integrated with an InGaAs/InAlAs HEMT transistor. MBE is used to first grow the multilayers for the HEMT, on top of which the InGaAs/InAlAs layers for the PIN is grown. The PIN photodetector layers are later etched away from the section which is used for the HEMT. The fabrication scheme is mostly similar to that

of example 1 except that in this case, the transistor layers are grown first and then the photodetector layers are grown on top instead of vice versa as in example 1. Similar to example 1, the growth is a single step process where a considerable number of layers are grown as the PIN photodetector and the HEMT do not share any layers, which adds to the complexity of the fabrication process. A cross sectional view of this photoreceiver is shown in Figure 2.5.

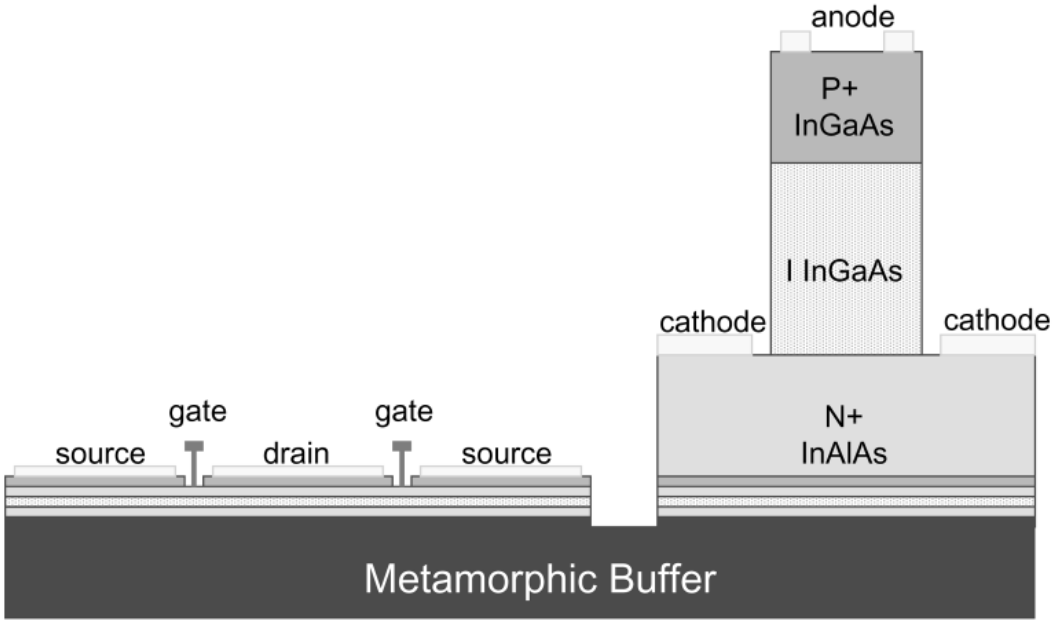


Figure 2.5: Cross-sectional view of the PIN/HEMT photoreceiver of Example 5 [84].

The unpackaged responsivity of the photodetector in this realization was measured to be 0.39 A/W at 1.55 um optical wavelength, from which the overall responsivity of the photoreceiver was calculated to be 210 V/W. The -3 dB bandwidth of the photoreceiver was measured to be 38 GHz which was improved to be 40 GHz with the use of a buffer amplifier.

2.2.6 Example 6: InAlAs/InGaAs WPD/HEMT Photoreceiver on InP substrate

In this realization [85], a waveguide photodiode (WPD) was monolithically integrated with an InGaAs/InAlAs HEMT transistor. The fabrication of this photoreceiver was done in a two-step process the first of which consisted of the growth of the photodetector and waveguide layers via MOVPE process while the second step consisted of the regrowth of the HEMT layers via MBE. Due to the twp step process, the fabrication process is considerably more complex compared to the other examples, especially the HBT common layer examples. The integration scheme of this photoreceiver is shown in Figure 2.6.

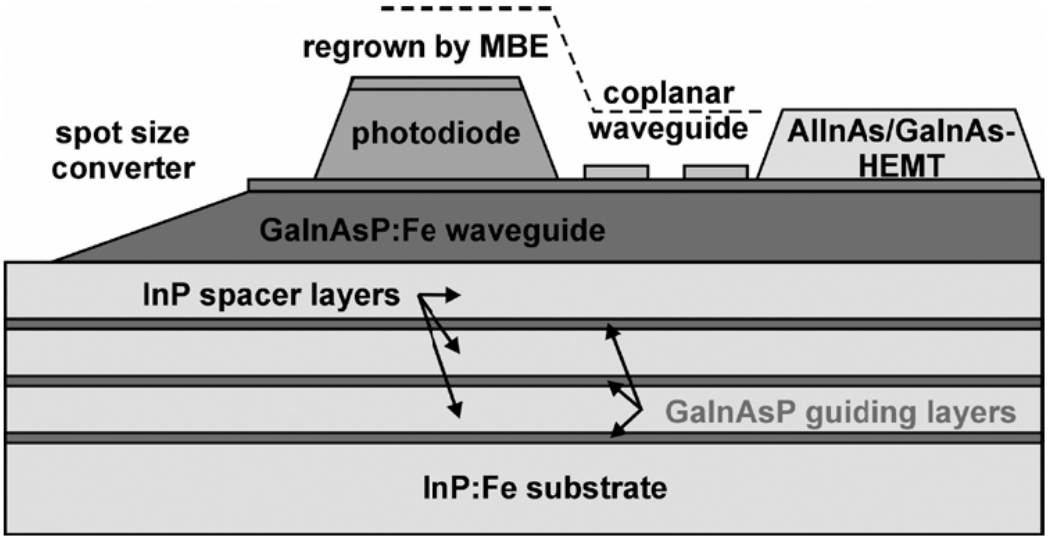
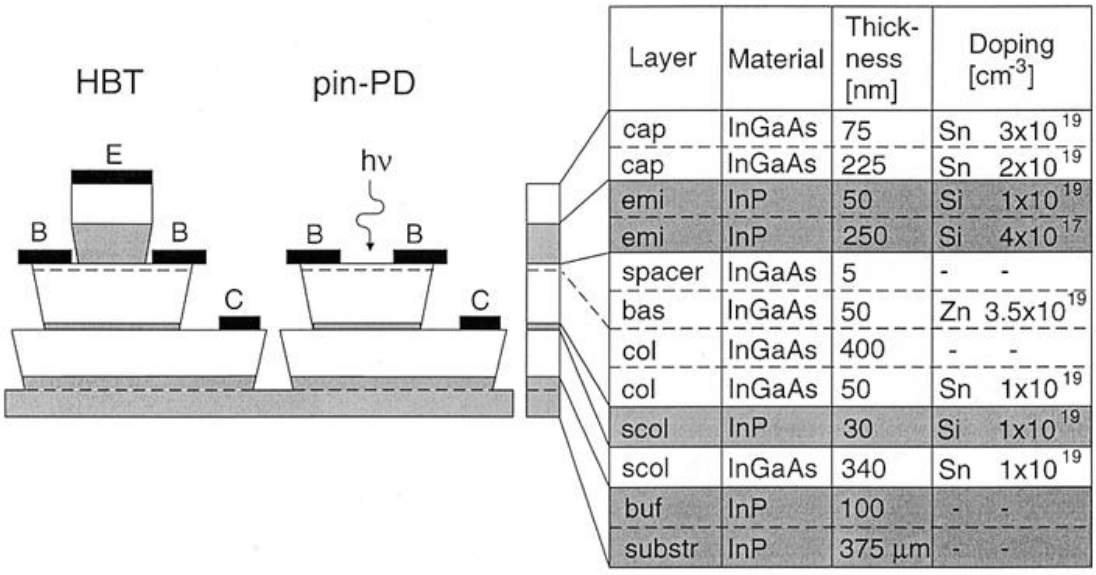


Figure 2.6: Integration scheme of the WPD/HEMT photoreceiver of Example 6 [85].

Using laser at wavelength 1.55 um, the -3 dB bandwidth of the photoreceiver was measured to be over 70 GHz. A photodiode DC responsivity of 0.64 A/W and an overall photoreceiver responsivity of 45.4 V/W was achieved from this realization.

2.2.7 Example 7: InGaAs/InP PIN/HBT Photoreceiver

In this realization [7], a top illuminated PIN photodiode was monolithically integrated with an InGaAs/InP HBT transistor. The fabrication scheme of this photoreceiver is similar to that of examples 3 and 4 in that the layers for the base and collector of the HBT are common with the layers of the photodetector. Similar advantages as examples 3 and 4 are also achieved in this case, i.e. the layer structure of both the



Layer	Material	Thick-ness [nm]	Doping [cm^{-3}]
cap	InGaAs	75	Sn $3x10^{19}$
cap	InGaAs	225	Sn $2x10^{19}$
emi	InP	50	Si $1x10^{19}$
emi	InP	250	Si $4x10^{17}$
spacer	InGaAs	5	- -
bas	InGaAs	50	Zn $3.5x10^{19}$
col	InGaAs	400	- -
col	InGaAs	50	Sn $1x10^{19}$
scol	InP	30	Si $1x10^{19}$
scol	InGaAs	340	Sn $1x10^{19}$
buf	InP	100	- -
substr	InP	375 µm	- -

Figure 2.7: Cross-sectional view of the PIN/HBT photoreceiver of Example 7 [7].

photodetector and the HBT is grown in a single step avoiding a regrowth process with its complexities, and the photodetector fabrication process is fully incorporated into the transistor fabrication. A similar disadvantage involving the speed-responsivity tradeoff also applies here. A cross sectional view of this photoreceiver is shown in Figure 2.7.

In this realization, a dark current value less than 2 nA (the PD being biased at -3V) and a DC responsivity value of 0.32 A/W were measured at wavelength 1.55 um for the photodiode, while bandwidth values of 34 GHz and 50 GHz were achieved for transimpedance gain values of 380Ω and 170Ω respectively.

2.2.8 Hybrid assembly

It was noted that hybrid assembly between a photodetector and an amplifier where the detector and transistors are not integrated on a single substrate, and instead the photodetector and amplifier are individually fabricated and later connected, are also known in the technology. However such an assembly was not considered in view of the fact that monolithic integration between the photodetector and transistors provides higher fabrication simplicity and ease of implementation as both the photodetector and the amplifier is fabricated at the same time in a single fabrication process and the design, modelling and implementation of complex external interconnection procedures between the photodetector and the amplifier elements requiring precision is not required unlike the hybrid assembly approach [110]. Traditionally, the hybrid assembly approach offered worse sensitivity, noise and speed performance compared to that of a monolithic integration of equivalent components [40] due to the parasitics of the interconnect between the photodetector and the amplifier elements. However, more recently, techniques were developed to compensate for or otherwise desensitize the effects of these parasitics and they were used to achieve excellent performance results with the hybrid assembly where a bandwidth of 39.3 GHz and a transimpedance gain of 1.3 kΩ of the transimpedance amplifier was achieved [109]. In spite of these results, the disadvantages of implementation complexities as mentioned above continue to exist, and the techniques to overcome the parasitics

impose design limitations such as the use of specific amplifier topologies [109]. In light of these drawbacks, the hybrid assembly approach was not chosen for this work.

2.3 COMPARISION AND SELECTION OF PHOTODETECTOR TECHNOLOGY

As previously mentioned, the focus of this research will be on the circuit design and transistor design of the preamplifier portion of the photoreceiver and not the photodetector. However, the selection of the photodetector is important because the type of photodetector that is selected will have important influences on design considerations in future chapters. As such, it is important that the selection of the photodetector is made with the objectives of the project in mind.

Edge illuminated photodiodes, which include waveguide photodiodes and travelling wave photodiodes as used in example 6 were considered in the first instance as they provide excellent trade-off capabilities between speed and quantum efficiency [41], which makes it possible to attain excellent bandwidth-efficiency product characteristics. In particular, waveguide photodiodes feature very high power capability due to a more uniform carrier distribution along the absorption region [42]. However, the downside of this option is that inputting the signal from the fibre to the waveguide structure of a waveguide photodiode generally caused much higher coupling losses compared to a traditional vertically illuminated photodiode [41], which in turn causes much lower absorption and poor efficiency. As such, these photodiodes are generally not used for low loss optical receivers.

Vertically illuminated photodiodes were considered next, which can be divided into two categories, namely the metal-semiconductor-metal (MSM) photodiode which is used in example 2 (discussed in subsection 2.2.2), and the PIN/avalanche photodiode which is used in examples 1, 3-5 and 7 (discussed in subsections 2.2.1, 2.2.3-2.2.5 and 2.2.7 respectively). The MSM photodiode makes an excellent candidate for use in high speed, i.e. high bandwidth OEIC circuits, and has an advantage over the PIN photodiode, as the MSM photodiode has a lower intrinsic capacitance per unit area compared to that of the PIN photodiode [41]. However, the downside of the MSM photodiode is that it has lower responsivity and higher dark current compared to a PIN photodiode of similar speed. On the other hand, the downside of the PIN photodiode, despite its much higher responsivity and quantum efficiency and low dark current, is that in order to operate at very high frequencies, its size must be made significantly smaller in order to account for the increasing capacitance of the intrinsic layer, which increases the alignment accuracy requirements. However, techniques have been developed to overcome this drawback in recent times [43], and TCAD simulations have been used to develop InP/InGaAs PIN photodiodes with superb DC and RF performance, with a cut-off frequency of 5.23 THz and a breakdown voltage of 34V at a $100A/m^2$ current density [44]. The primary advantage of selecting the PIN photodetector, particularly for this work, is the compatibility between the layers of the PIN photodetector and the HBT due to the Base, Subcollector and Collector layers of the HBT being respectively common with the P-type, Intrinsic and the N-type layers of the PIN photodiode as observed in examples 3, 4 and 7, which allows for monolithic integration of the photodiode and the HBTs on a single chip [7, 12]. For example, Figure 2.7 depicts such a monolithic integration of an InP/InGaAs HBT and an InP/InGaAs PIN photodiode from a past work [7]. Such single step common layer

monolithic integration is undoubtedly preferable to a two/multiple step fabrication process such as example 6 or a lengthy single step process such as examples 1 and 5, due to the significantly simpler fabrication procedure of the monolithic integration, resulting in a significantly lower mass production cost. In consideration of the above points, the PIN photodiode was selected for this work. The advantages and disadvantages of the various types of photodiodes as discussed in this section are summarized in Table 2.1.

TABLE 2.1
SUMMARY OF ADVANTAGES AND DISADVANTAGES OF VARIOUS TYPES OF PHOTODIODES

Photodiode type	Subcategories	Advantages	Disadvantages
Edge illuminated photodiodes	Waveguide photodiodes	Excellent bandwidth-efficiency product characteristics and very high power capability due to a more uniform carrier distribution along the absorption region.	Much higher coupling losses from the fibre to the photodiode structure.
	Travelling Wave photodiodes		
Vertically illuminated photodiodes	Metal-Semiconductor-Metal (MSM) photodiodes	Suitable for high speed applications due to low intrinsic capacitance per unit area.	low responsivity and high dark current compared to the PIN photodiode.
	Avalanche/PIN photodiodes	Higher responsivity and quantum efficiency, low dark current and compatibility between the layers of a PIN photodetector and a HBT.	Relatively high capacitance of the intrinsic layer.

2.4 COMPARISION AND SELECTION OF TRANSISTOR TECHNOLOGY

Some of the many transistor types known in the field of technology are, BJT, MESFET, MOSFET, JFET, HBT, HEMT, etc. However, because a high bandwidth is

one of the requirements of the amplifier in our intended application, the chosen transistor type will be required to be capable of high speed operation. Military radars generally use the L, S, C,X, K_u, K and K_a IEEE radar bands which span from 1 GHz to 40 GHz [86]. As such, we begin by short listing the transistor types that are capable of high speed operation, namely the HEMT (High Electron Mobility Transistor) and HBT (Heterojunction Bipolar Transistor). The two short listed transistor types are briefly discussed as follows.

2.4.1 HEMT (High Electron Mobility Transistor)

The high electron mobility transistor (HEMT), also known as the heterojunction field effect transistor (HFET) or modulation-doped field effect transistor (MODFET), is a field effect transistor which features a heterojunction (which is known as a junction of two materials with different band gaps) as the channel instead of a doped region, which is usually the case for a regular MOSFET. HEMT transistors are able to operate at much higher frequencies than ordinary transistors, up to millimeter wave frequencies, and are used in high frequency products such as cell phones, satellite television receivers, and radar equipment.

2.4.1.1 Technical difference from regular homojunction FETs

In regular field effect transistors, mobile electrons are generated in the channel from impurities, which are introduced to semiconductors in order to allow conduction. However, the generated electrons collide with the same impurities used to generate them, which result in a relatively slow electron flow. This is prevented from taking place in a HEMT through the use of a heterojunction of a highly doped wide-bandgap n-type donor-supply layer and an undoped narrow-bandgap channel layer, which

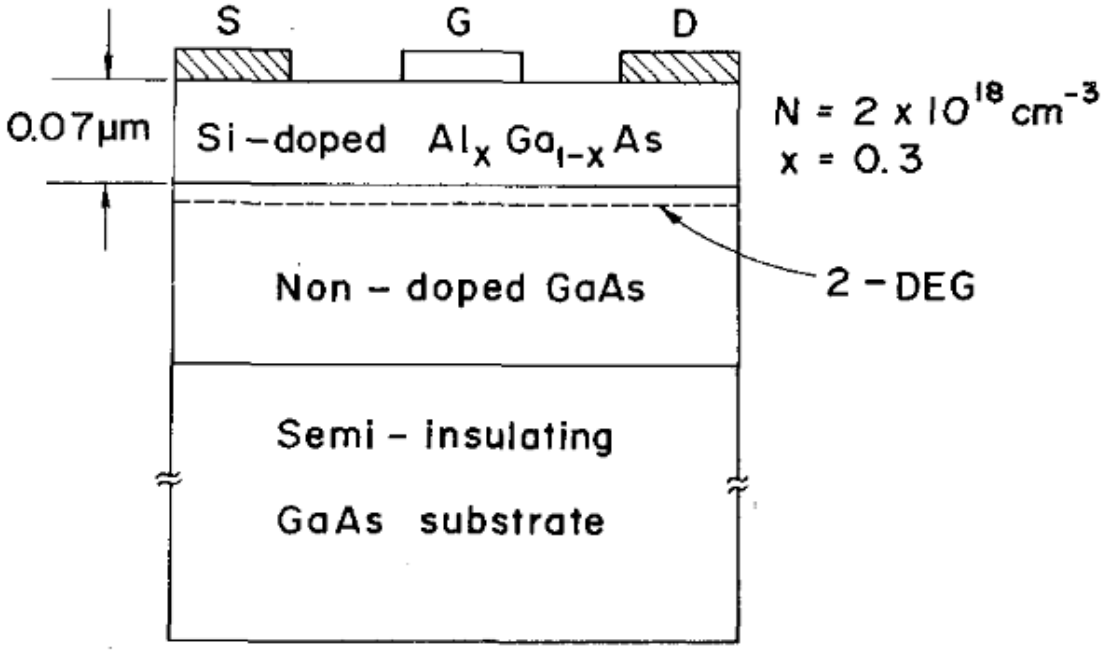


Figure 2.8: Cross-sectional view of a HEMT in Depletion-mode[87].

results in the generation of high mobility electrons. Electrons generated from the impurities in the thin and heavily doped donor supply layer diffuse to the undoped channel layer, thereby forming a depletion layer and a quantum well is formed within the undoped layer in which electrons are able to flow without any collision with impurities, as they are absent in the undoped layer. Thus a very thin channel is formed in which a very high concentration of electrons can flow with very low resistance at ultra high speeds, and such a layer is known as a two-dimensional electron gas (2DEG) layer. Application of voltage to the gate however influences the channel resistance the same way as a regular field effect transistor. Thus the HEMT is capable of very high (RF) frequencies [90, 91].

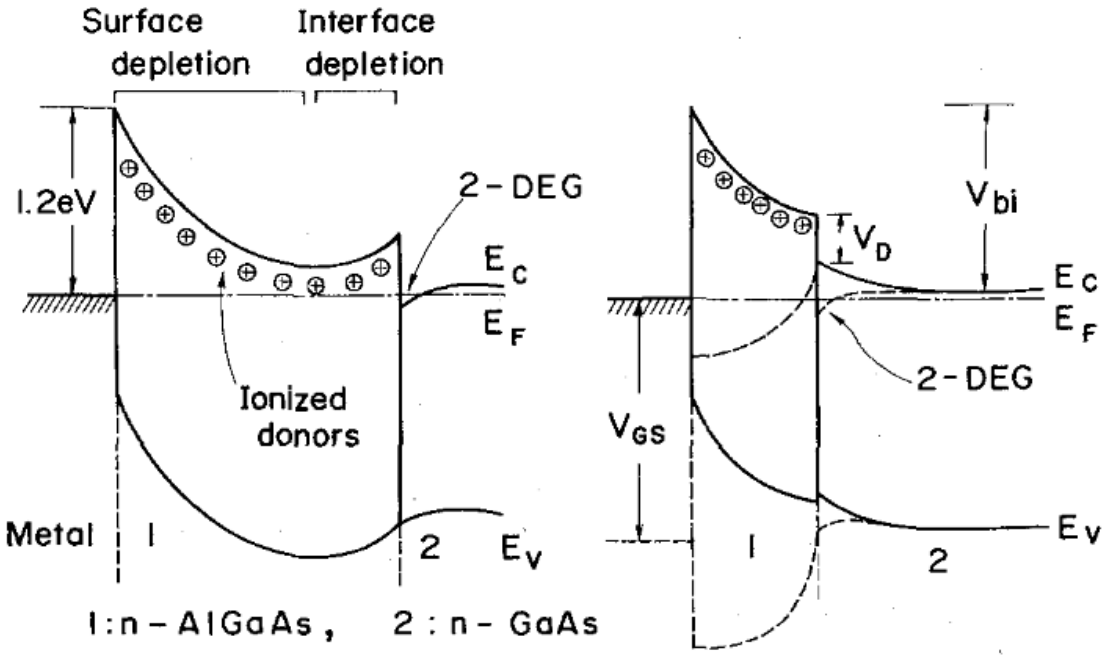


Figure 2.9: Energy-band diagram of a HEMT in (a) Depletion-mode (b) Enhancement-mode [87].

2.4.1.2 Fabrication procedure

The fabrication procedure of an AlGaAs/GaAs HEMT is discussed here as an example. However, similar procedures are also known for InAlAs/InP HEMTs. Figure 2.8 shows the cross sectional view of a HEMT (in Depletion-mode) which comprises a selectively doped AlGaAs/GaAs heterojunction structure. An undoped GaAs layer and Si-doped n-type AlGaAs layer are successively grown on a semi-insulating GaAs substrate by Molecular Beam Epitaxy (MBE). Due to a higher electron affinity of GaAs, free electrons in the AlGaAs layer are diffused to the undoped GaAs layer, where they form a high-mobility two-dimensional electron gas (2DEG) along the interface. Figure 2.9(a) and 2.9(b) shows the energy-band diagram of a HEMT in Depletion-mode and Enhancement-mode respectively in an unbiased state.

2.4.1.3 Operating principle

Depletion-mode

In Depletion-mode, the n-type AlGaAs layer of the HEMT is fully depleted when free electrons are trapped by surface states and electrons are diffused into the undoped GaAs area. The Fermi level of the gate metal is matched to the pinning point, which is 1.2 electron volts below the conduction band. Due to the reduced AlGaAs layer thickness, the electrons supplied by donors in the AlGaAs layer becomes insufficient to pin the surface Fermi level. As a result, the space charge region extends into the undoped GaAs layer and, consequently, band bending results in the upward direction, and the two-dimensional electron gas is deactivated, as observed in Figure 2.9(a) [87].

Enhancement-mode

When a positive gate-source voltage V_{GS} higher than the threshold voltage is applied to the gate, electrons accumulate at the interface and form a two-dimensional electron gas, as indicated by the dashed lines in Figure 2.9(b). Thus, the HEMT enters Enhancement-mode and a high-speed conductive channel between the drain and the source terminals is activated.

2.4.2 HBT (Heterojunction Bipolar Transistor)

The heterojunction bipolar transistor (HBT) is a type of bipolar junction transistor that uses different semiconductor materials for the emitter and base regions, thereby forming a heterojunction. The advantage of the HBT over the BJT is that it can handle signals of very high frequencies, up to several hundred GHz. It is generally used in modern ultra high speed circuits, typically radio-frequency (RF) systems, and in

applications requiring a high power capability, such as RF power amplifiers in cellular phones [92, 91]. Incidentally, high power capability is a very important consideration in this work because the amplifier in our target application (i.e. radar for electronic warfare) would be required to handle a very broad dynamic power range, ranging from low power levels to very high power levels.

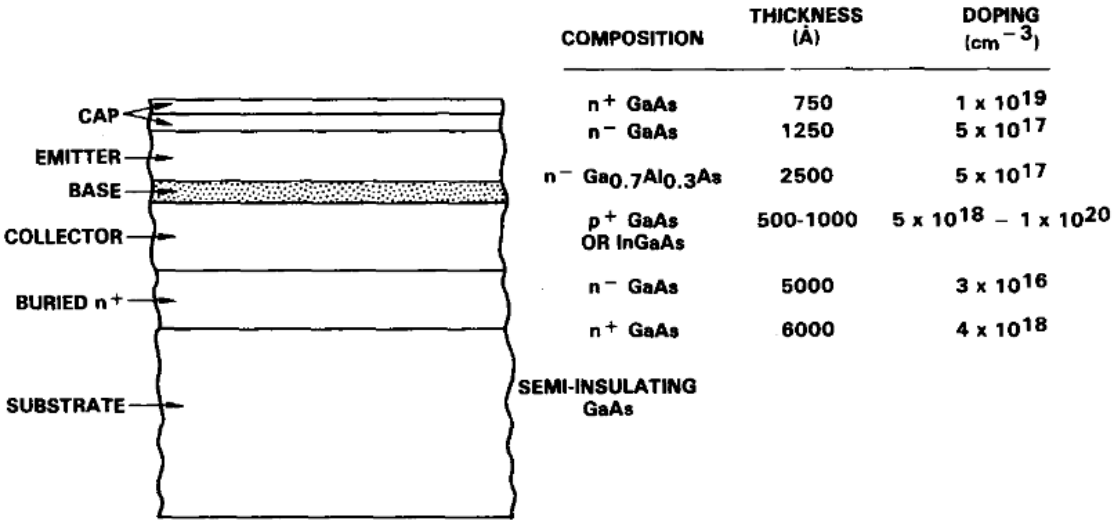
2.4.2.1 Technical difference from regular BJTs

The main difference between the HBT and the regular bipolar junction transistor is the use of different semiconductor materials for the emitter-base junction, forming a heterojunction. The resulting effect of the heterojunction is that it minimizes the injection of holes from the base into the emitter region, as the potential barrier in the valence band is higher than in the conduction band. Unlike in a regular bipolar junction transistor, this makes it possible to use a high doping density in the base, causing the base resistance to decrease while retaining the gain.

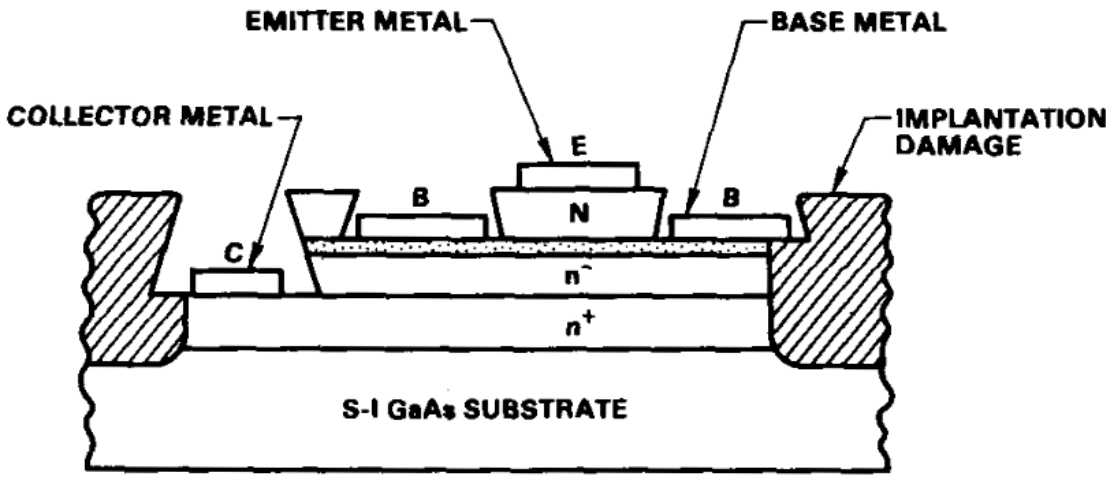
2.4.2.2 Fabrication procedure

Epitaxial technologies that are generally used for fabrication of the HBT are MBE and MOCVD and more recently MOVPE. All of these technologies are capable of growing highly pure epitaxial layers with decent crystalline perfection, highly controlled doping levels higher than 10^{19} impurities per cm^3. These technologies are also capable of achieving highly controlled changes in doping level during growth with minimal adjustment in growth parameters. The doping may be varied gradually or abruptly. Furthermore, in all three techniques, a change in semiconductor, i.e. a change in energy gap during growth is reasonably easy to achieve, which enables the growth and fabrication of heterojunctions. Lastly, in all of these techniques, the layer

thicknesses can be controlled with excellent accuracy, and extremely thin layers are realizable. One of these techniques is used to grow the epitaxial layers of HBTs. The epitaxial layers of an example HBT, which is a GaAlAs/GaAs HBT is shown in Figure 2.10(a). Once the layers shown in the figure are grown, techniques such as masking and photolithography are used to etch away the layers as necessary to achieve the final HBT structure as shown in Figure 2.10(b). Although the example in



(a)



(b)

Figure 2.10: Example GaAlAs/GaAs HBT (a) epitaxial layer structure (b) Cross-sectional view [87].

the figure is a GaAlAs/GaAs HBT, a similar technique is also used for the fabrication of HBTs of other materials, such as SiGe/Si, InGaAs/InP, etc.

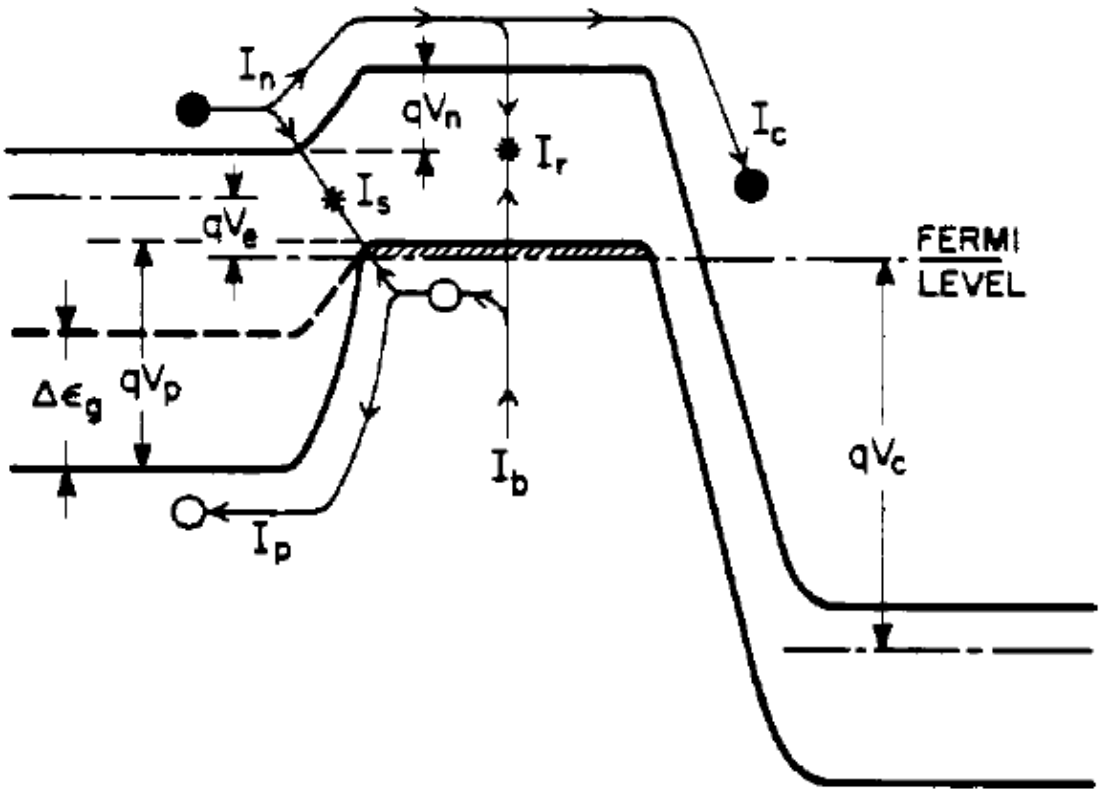


Figure 2.11: Energy-band diagram of a HBT [89].

2.4.2.3 Operating principle

Figure 2.11 shows the energy-band diagram for a HBT [89]. The net currents of the emitter, base and collector terminals of the HBT, I_e, I_b and I_c respectively can be expressed as follows:

$$I_e = I_n + I_p + I_s \tag{2.1}$$

$$I_b = I_p + I_r + I_s \tag{2.2}$$

$$I_c = I_n - I_r \tag{2.3}$$

where,

I_n is a current of electrons injected from the emitter into the base, I_p is a current of holes injected from the base into the emitter, I_s is a current due to electron-hole recombination within the forward biased emitter-base space charge layer and I_r is a current lost from I_n due to bulk recombination.

Therefore the current gain of the HBT can be expressed as follows:

$$\beta = I_c/I_b = (I_n - I_r)/(I_p + I_r + I_s) \tag{2.4}$$

Therefore the maximum current gain of the HBT is expressed as follows:

$$\beta_{max} = I_n/I_p = J_n/J_p \tag{2.5}$$

where J_n and J_p are electron and hole injection current densities respectively.

The electron and hole injection current densities can be expressed as follows based on PN junction theory:

$$J_n = N_e * v_{nb} * \exp(-qV_n/kT) \tag{2.6}$$

$$J_p = P_b * v_{pe} * \exp(-qV_p/kT) \tag{2.7}$$

where,

N_e and P_b are uniform doping levels of the emitter and base respectively, v_{nb} and v_{pe} are the mean speeds of the electrons at the emitter end of the base and holes at the base end of the emitter respectively, and qV_n and qV_p are the heights of the potential energy barriers for electrons and holes respectively.

If the energy gap of the emitter is larger than the energy gap of the base by $\Delta\varepsilon_g$ due to the heterojunction between the emitter and the base, then,

$$\Delta\varepsilon_g = q(V_p - V_n) \tag{2.8}$$

From equations 2.5, 2.6 2.7 and 2.8, we get,

$$\beta_{max} = J_n/J_p = N_e/P_b * v_{nb}/v_{pe} * \exp(\Delta\varepsilon_g/kT) \tag{2.9}$$

The value of the term v_{nb}/v_{pe} generally varies between 5 and 50. Therefore from equation 2.9, we conclude that in order to achieve a β_{max} value equal to or greater than 100, which is a requirement for a decent transistor, at least one of the two following conditions must be met:

Condition 1: $N_e >> P_b$

Condition 2: $\Delta\varepsilon_g$ is at least a few times that of kT.

For regular homojunction BJT transistors, $\Delta\varepsilon_g = 0$ as there is no difference between the energy bandgaps for the base and the emitter, and as such, condition 2 cannot be met. Therefore Condition 1 remains the only option, due to which the base doping has to be made significantly lower compared to the emitter doping. This significantly limits the speed and high frequency operation of the transistor.

However, for HBTs, Condition 2 becomes an available option as a result of which the constraint of Condition 1 no longer applies. In other words, a high base doping becomes an option, which significantly improves the speed and high frequency operation of the transistor.

2.4.3 Comparison of HEMT and HBT in Light of the Objectives of this Work

In terms of bandwidth, both technologies meet our requirements (at least up to K_a IEEE radar bands) with ease and are capable of achieving photoreceiver bandwidths of over 50 GHz [8, 9]. However, in terms of other important figures of merit, they differ in performance and strengths, as detailed as follows.

2.4.3.1 Arguments in favour of Selecting HEMT Technology for this Work

Noise performance of HEMTs is generally better than HBTs especially at high frequencies [7, 28, 29, 30].

Since one of the required figures of merit of the amplifier is a very broad RF bandwidth (as explained in section 1.3), one possibility is to use a distributed amplifier which is known for its exceedingly high bandwidth performance. If that approach is taken, the HEMT offers advantages over the HBT because the distributed amplifier is more difficult to implement using HBTs compared to HEMTs due to the resistive small signal behaviour of the base-emitter junction of HBTs. Bandwidths of over 100 GHz have been achieved via HEMT distributed amplifiers [26]. The merits of the distributed amplifier approach compared to other approaches in light of the requirements of this work are discussed in more detail in chapter 3.

2.4.3.2 Arguments in favour of Selecting HBT Technology for this Work

The minimum gate width of a HEMT is much lower than the emitter width of a comparable HBT [7]. As such, the HBT has a major advantage in terms of fabrication simplicity.

The gate threshold voltage variation of HEMT's is greater than the base-emitter voltage variation of bipolar junction transistors and HBTs. Therefore bias-point control of HEMT-based circuits is typically more difficult [7].

For certain semiconductor material options such as SiGe used with Si, AlGaAs used with GaAs and InP used with InGaAs (see examples 4, 3 and 7 respectively in section 2.2) the same epitaxial layers can be shared by both the photodetector (a PIN photodiode) and the base-collector layers of the HBT, thereby considerably simplifying the fabrication process [27]. This option is only available for HBTs, in particular, SHBTs, and not available for HEMTs.

HBTs are advantageous for high dynamic range applications due to inherently high linearity and low 1/f noise [31].

TABLE 2.2
SUMMARY OF ADVANTAGES AND DISADVANTAGES OF SELECTING EACH OF THE HEMT AND THE HBT FOR THIS WORK.

Transistor type	Advantages	Disadvantages
High Electron Mobility Transistor (HEMT)	• Better noise performance. • Better compatibility with distributed amplifiers.	• Relatively higher gate threshold voltage variation. • Relatively complex fabrication process.
Heterojunction Bipolar Transistor (HBT)	• Fabrication simplicity. • Easier control of bias point. • Epitaxial layers of the base and collector layers can be shared with that of a PIN photodetector. • Superior linearity characteristics.	• Worse noise performance. • Relatively complex implementation with distributed amplifiers due to the resistive small signal behaviour of the base-emitter junction.

2.4.4 Final Selection of Transistor Technology and Justification

The advantages and disadvantages of each of HEMT and HBT discussed in section 2.4.3 are summarised in Table 2.2. As can be observed, the only advantages that the

HEMT has over the HBT in light of our selection criteria is its better overall noise performance and its ease of implementation in a distributed amplifier. However, in recent times, HBT amplifiers have been successfully made to produce noise figures comparable to their HEMT counterparts [29]. With regards of ease of implementation in distributed amplifiers (which may be desirable in this work due to their high bandwidth performance and gain-bandwidth product), even though HEMTs have a clear advantage, high performance distributed amplifiers employing HBTs have been realized very successfully as of late via a technique wherein multiple HBTs in a cascode formation is used in each gain stage instead of a single transistor [12].

Furthermore, in terms of linearity, which is the primary focus of this work, and fabrication simplicity, the HBT clearly has an advantage over the HEMT. As such, in view of all the aforementioned pros and cons of both transistor technologies, the HBT is chosen for use in this work.

2.5 SELECTION OF SEMICONDUCTOR MATERIALS

Materials that are commonly used for the substrate of HBTs in the photoreceiver context are silicon (Si), gallium arsenide (GaAs), and indium phosphide (InP). With these substrate materials, silicon (Si) with silicon-germanium alloys (SiGe), aluminium gallium arsenide (AlGaAs) with gallium arsenide (GaAs), and indium phosphide (InP) with indium gallium arsenide (InGaAs) are used for the epitaxial layers respectively. See section 2.2 for examples of past realizations of photoreceivers using each of these semiconductor technologies (see examples 3, 4 and 7 discussed in section 2.2).

2.5.1 Comparison of Transistor Semiconductor Technologies

The pros and cons of the various material and epitaxial options for the HBT are discussed as follows:

2.5.1.1 Arguments in favour of using Si with SiGe in this work:

Speeds up to 77 GHz have been achieved with SiGe technology [32]. Unity current gain cut-off frequencies (f_t) of 350 GHz with SiGe HBTs have been reported [35].

SiGe has the best noise performance of the three technologies [34].

2.5.1.2 Arguments in favour of using GaAs with AlGaAs in this work:

GaAs HBT speeds are comparable with that of the other two options with unity current gain cut-off frequencies (f_t) of 171 GHz and oscillation frequencies (f_{max}) of 275 GHz having been reported [37, 38].

The largest advantage of GaAs HBT technology lies in its high power handling capability due to its very high breakdown voltage, BV_{CEO}, which is usually greater than 10V [39]. On the other hand, limited power handling capacity is the main limitation of SiGe based HBTs with BV_{CEO} values typically less than 3V, and even lower when configured for higher f_T values [39]. This makes SiGe HBTs unsuitable for use in this work despite their excellent noise performance, as a low power handling capacity would generally mean low dynamic range.

2.5.1.3 Arguments in favour of using InP with InGaAs in this work:

HBT transistor unity current gain cut-off frequencies (f_t) greater than 710 GHz have been achieved with InP/InGaAs technology [33, 36].

InP HBTs feature decent BV_{CEO} values and power handling capabilities, which are sufficient for this work, although inferior to those of GaAs HBTs [34, 39].

As previously mentioned, HBTs made of InP/InGaAs are also ideal for monolithic optoelectronic integrated circuits as their base-collector-subcollector layers are common with the layers of a PIN-type photodetector, which contributes significantly to fabrication simplicity [7]. Additionally, it has been shown in past work that such monolithic integration produces superior results (lower noise and higher photodetector sensitivity i.e. higher photodetector speed) compared to the alternative, i.e. a hybrid assembly [40].

$In_xGa_{1-x}As$ (where x=0.53) has a bandgap energy of 0.75 eV, which is compatible with photodetection at 1.55 um optical wavelength. On the other hand, the bandgap energy values for Si and GaAs are 1.12 eV and 1.43 eV respectively. As a result, photodetectors based on SiGe/Si and AlGaAs/GaAs are photosensitive to optical wavelength around 0.85 um. This causes photodetector systems using InGaAs/InP materials to have significantly less attenuation compared to photodetector systems using SiGe/Si or AlGaAs/GaAs, as the attenuation in optical fibres is 2 dB/km when the optical wavelength is 85 um, while the attenuation is only 0.2 dB/km when the optical wavelength is 1.55 um [93].

TABLE 2.3
BANDGAP ENERGY AND APPLICABLE SPECTRAL RANGE FOR VARIOUS MATERIALS USED IN THE CONSTRUCTION OF PHOTODETECTORS [93]

Material	Si	GaAs	$In_xGa_{1-x}As$
Bandgap (eV)	1.12	1.43	0.75
Optical wavelength (λ)	0.5-0.9	0.75-0.85	1.3-1.65

2.5.2 Final Selection of Transistor Semiconductor Technology (Materials) and Justification

In terms of photodetection, InP/InGaAs is the best option as it has the best optical fibre attenuation characteristics of the three options due to its compatibility with 1.55 um optical wavelength which correspond to a fibre attenuation of only 0.2 dB/km as opposed to a fibre attenuation of around 2 dB/km resulted from the other two options, as discussed in more detail subsection 2.5.1.3. It is also observed from the above discussions that InP/InGaAs HBTs is the clear winner of the three options in terms of transistor speed (i.e. bandwidth) as well. This material formation is also the clear choice in terms of fabrication simplicity. Table 2.4 shows a published comparison of various figures of merit of HBTs of the three semiconductor technologies, at the same base current (similar bias) [34]. As can be observed from Table 2.4, although the noise performance of the InP HBT is inferior to that of the SiGe HBT by about 1 dB, it is significantly superior to that of the GaAs HBT, which is observed to have the worst noise performance of the three. As the noise performance is an important consideration of this work, the GaAs HBT is considered unsuitable for this work in light of the availability of InP HBTs. It is also observed that the GaAs HBT has the lowest β gain value. As already discussed, the SiGe HBT is also considered

unsuitable for this work due to its very low breakdown voltage BV_{CEO} value. This leaves the InP HBT as the only logical option which is found to be the most balanced performer in light of the requirements of this project. The main drawback is its high cost. However, this drawback is outweighed by its benefits and its particular suitability for this work.

TABLE 2.4
COMPARISON OF AlGaAs/GaAs HBT, Si/SiGe HBT AND InGaAs/InP HBT FOR DIFFERENT FOMS [34]

Device	I_B (uA)	β at I_B=100uA	f_T (GHz)	f_{max} (GHz)	NF_{min} (dB)
AlGaAs/GaAs HBT	100	25	95.70	151.7	5.026
Si/SiGe HBT	100	51	278	134.6	1.748
InGaAs/InP HBT	100	40	302.6	416.6	2.735

2.6 CONCLUSION

The photodetector technology, transistor technology and the semiconductor materials that will be used in this work have been carefully selected from among multiple possible options for each category that have been used in past photoreceiver realizations. Justification for each selection was presented and discussed in detail. As can be observed, each selection is made with the goals of the project, as specified and established in Section 1.3 in detail, in mind, and the pros and cons of all options in each selection category are considered in light of these goals. The PIN photodetector, HBT transistor and the InP/InGaAs semiconductor combination were chosen for use in this work as the photodetector, transistor and semiconductor technologies respectively.

Chapter Three:

Comparison of Amplifier Topologies

3.1 INTRODUCTION

This chapter aims to answer the two research questions stated under "Objective 2" in Section 1.3, which are repeated as follows for the readers convenience:

1. Are the current feedback-based circuit designs optimal for maximising dynamic range performance?

2. Are other amplifier topologies capable of providing superior performance?

These questions are tackled through the analysis of circuit topologies that are potentially applicable for use for the design of the transimpedance amplifier, followed by an investigation and determination of the circuit topology from among the candidates that is best suited for use in this work with respect to the goals of the project.

For the analysis we have selected three popular transimpedance amplifier circuit topologies for comparison. A representative single heterojunction InP/InGaAs HBT [45] was used in all three circuits, so that the performance of the various circuit topologies could be compared. The Agilent Advanced Design System [14] was then used to simulate the noise, gain, gain compression and intermodulation performance of the three transimpedance amplifier topologies. Results are presented enabling comparison of the performance of the three amplifier topologies. Notably, these results were presented at the Asia Pacific Microwave Conference 2009 partly sponsored by the IEEE Microwave Theory and Techniques Society and the IEEE Antennas and Propagation Society, and led to a publication titled "*A comparison of InP HBT transimpedance amplifier topologies for high dynamic range photonic links*" in the proceedings of the conference.

3.2 CIRCUIT TOPOLOGIES

Although there may be a number of different amplifier configurations that are used and would be usable in OEIC photoreceiver applications such as in this work, three specific amplifier configurations were chosen as candidate for comparison and

analysis for this work as the authors found these three topologies to be among the most popular and most commonly used in such applications [7, 12, 25, 46]. The three transimpedance photoreceiver amplifier circuit topologies investigated in this work are briefly described as follows. In all cases, the PIN photodiode has been replaced by an ideal current source.

3.2.1 Shunt-series Transimpedance Amplifier

The first transimpedance amplifier topology considered is a simple two-stage design, employing shunt feedback on the first stage and series feedback on the second stage. The circuit structure is shown in Figure 3.1.

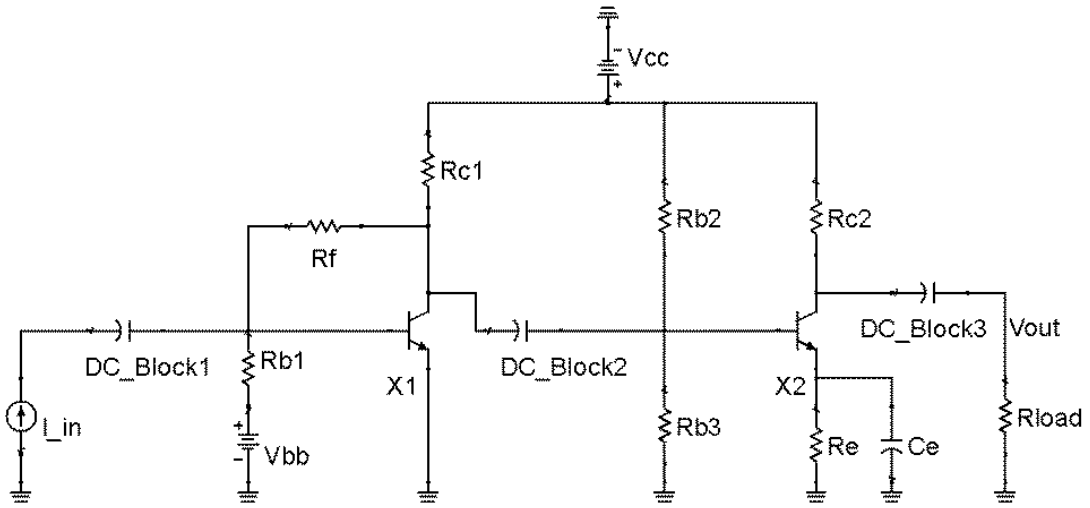


Figure 3.1: Shunt-series transimpedance amplifier topology.

This circuit topology was originally reported by Chieng and Minasian [46]. Separate local feedback has been applied to each stage rather than overall shunt feedback across both stages, as is typically the case with most transimpedance amplifier circuit designs [7, 94]. The reason for the local feedback loops rather than a single overall

feedback loop is to minimize loop delay and phase shifts between the amplifying stages and thereby improve stability [46].

3.2.2 Feedback Transimpedance Amplifier with Common-Base Input Stage

This topology was proposed by Vanisri and Toumazou [47]. It is also essentially a 2-stage design, however it features a single shunt feedback loop. Its main feature is that it has an additional common-base input stage, which provides optimal drive capability; that is high gain, high bandwidth and improved stability and noise performance. It is one of the common topologies used in optoelectronic transimpedance preamplifiers at present [7, 49]. This circuit is shown in Figure 3.2. Transistors X5, X6, X7 and X8 in Figure 3.2 are acting as level shifting diodes.

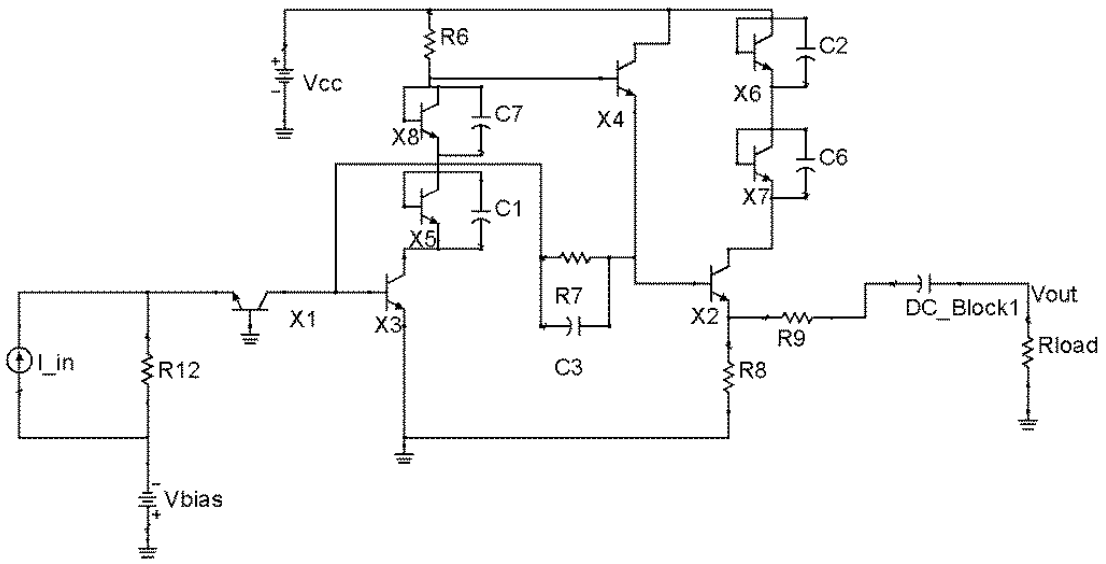


Figure 3.2: Transimpedance amplifier with common-base input stage.

3.2.3 Distributed Amplifier Employing Negative Resistance

Distributed amplifiers are potentially capable of gain bandwidth products that are very close to the product of the gain and the f_{max} of the transistor being used [13]. The

design of HBT distributed amplifiers is somewhat more complex than for HEMT distributed amplifiers, however, because of the input impedance characteristics of HBTs. HEMTs have input impedance characteristics that are very close to a series R-C, where the series resistance is quite small. HBTs on the other hand, have a forward-biased PN junction between the base and emitter, so the input resistance is much more significant. This typically leads to an increased attenuation on the input transmission line of the distributed configuration.

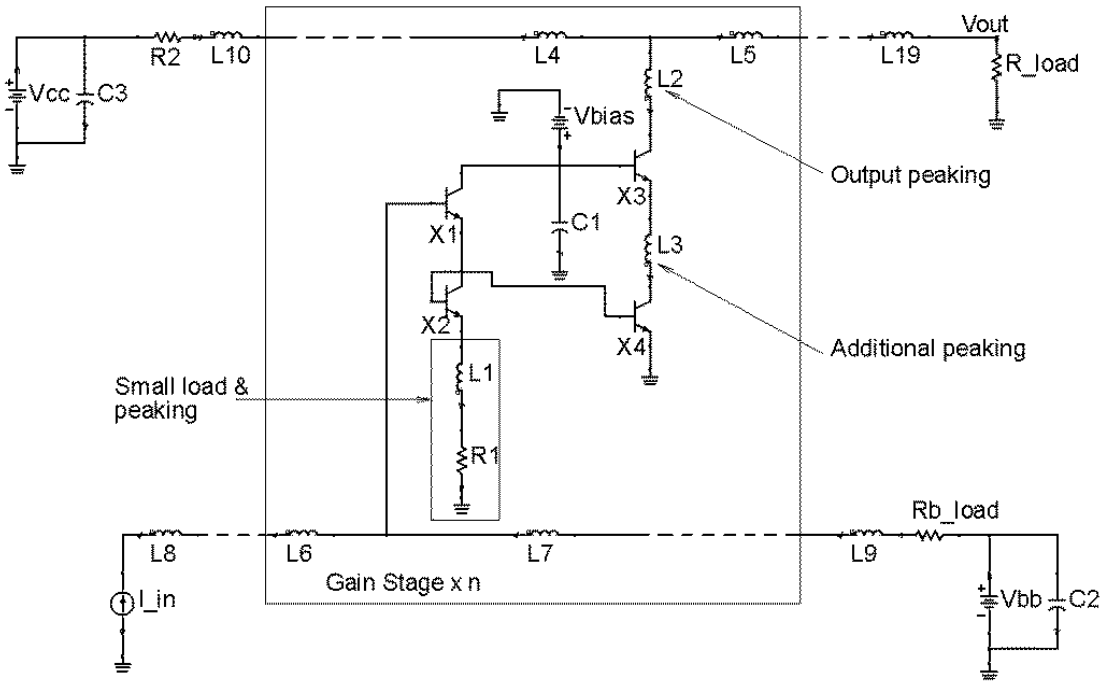


Figure 3.3: Schematic circuit of a single stage of Cohen's HBT distributed amplifier.

The transimpedance HBT distributed amplifier topology selected is that reported by Cohen *et al.* [25]. In Cohen's design, a gain stage as shown in Figure 3.3 is used in place of a single HBT. This amplifier is a refinement of that reported by Kobayashi *et al.* [50], where the resistive load on the input emitter follower stage has been replaced by a diode (X2) and a small resistive load with inductive peaking (R1 and L1).

Each gain stage comprises an input emitter-follower stage followed by a cascode connection of two HBTs. The cascode connection provides increased bandwidth by reducing the Miller capacitance compared with a simple common-emitter stage. It also increases the output shunt resistance, thereby reducing the attenuation on the output transmission line. The emitter-follower input stage acts as an active impedance transformer and generates an overall input impedance for the stage that exhibits capacitance and negative resistance. The negative resistance can be used to compensate for the attenuation on the input line due to the loss in the inductances. In addition, inductors L1, L2 and L3 are used for gain peaking to extend the bandwidth of the gain stage. A total of 4 gain stages were used in the complete distributed transimpedance amplifier.

3.3 COMPARISION METHODOLOGY

This section describes in detail the conditions under which the three amplifier circuit topologies were compared. Firstly, the same InP HBT transistor was used in each of the circuits. The transistor is an InP/InGaAs single heterojunction HBT, the large signal model for which was reported by Kim and Yang [45] and implemented in the Agilent ADS software [14].

3.3.1 Transistor Simulation Setup

A large signal equivalent circuit model ADS schematic for the transistor developed and discussed by Kim and Yang [45] is shown in Figure 3.4, along with its extracted large signal model parameter values. This schematic is basically a re-creation of the

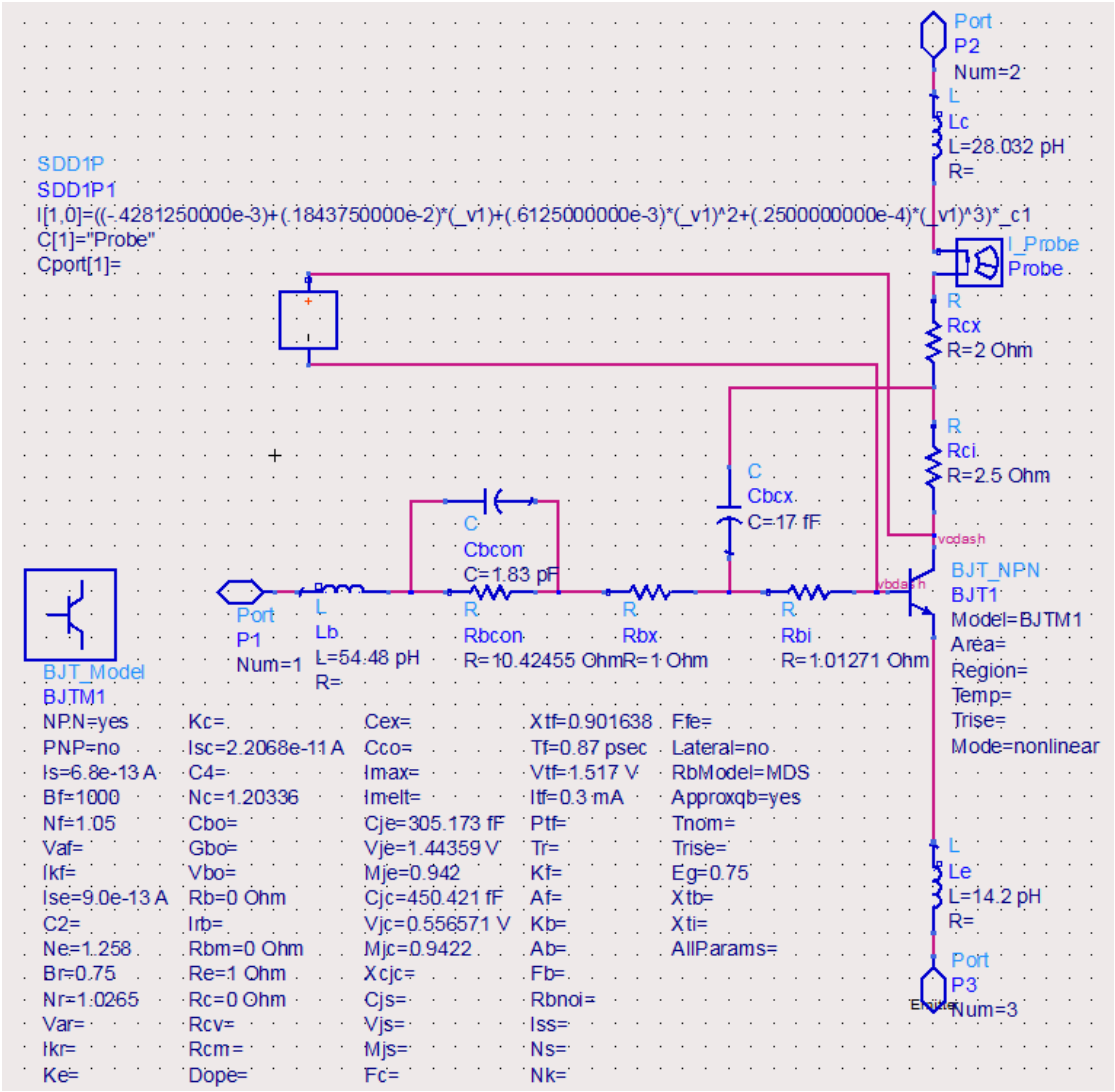


Figure 3.4: Large signal equivalent circuit model ADS schematic and the large signal model parameter values for the transistor referenced from [45].

large signal equivalent circuit model of the transistor shown in Figure 1 of [45], which is represented in Figure 3.5 in this work. Notably, the voltage source ($V_{J,T}$) used to model the reduction of emitter junction built-in potential and the temperature dependence of impact ionization as shown in this figure is omitted from our simulations, and instead, the current source $I_{CB}(V_{C'B'},I_C,T_j)$ is appropriately adjusted by using the graph shown in Figure 2 of [45] (which is represented in Figure 3.6 in this work) to solve the polynomials in equations (3) and (4) of [45], which are stated below as equations 3.1 and 3.2 respectively.

$$M(V_{C'B'},T_j) - 1 = a_0(T_j) + a_1(T_j)V_{C'B'} + a_2(T_j)V_{C'B'}^{\ 2} + a_3(T_j)V_{C'B'}^{\ 3} \quad (3.1)$$

$$I_{CB}(V_{C'B'},I_C,T_j) = |M(V_{C'B'},T_j) - 1|\, I_C \quad (3.2)$$

where, (*M-1*) is the impact ionization multiplication factor,

T_j is the junction temperature, and

$a_i(T_j)$ where (i = 1, 2, 3) are empirical terms used to empirically model the positive dependence of the impact ionization multiplication factor on the reverse bias voltage across the base-collector junction, V_{CB} and junction temperature.

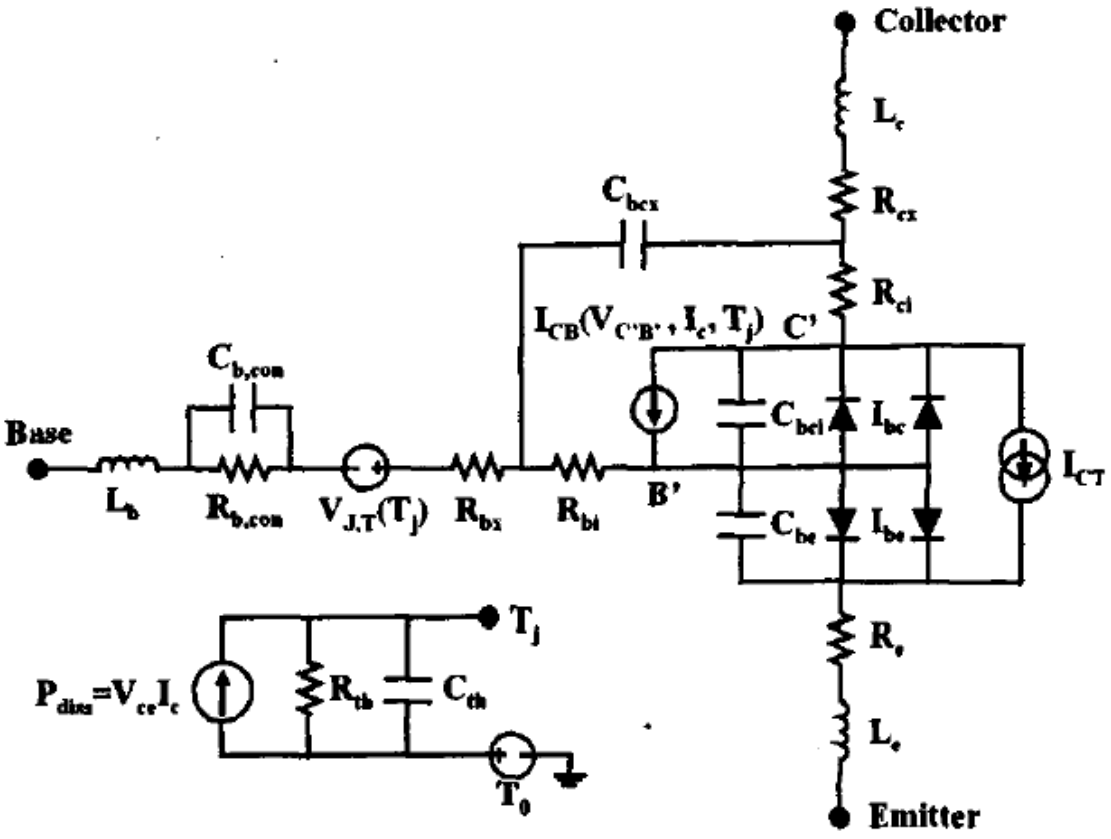


Figure 3.5: Large-signal equivalent circuit model of the InP/InGaAs SHBT [45].

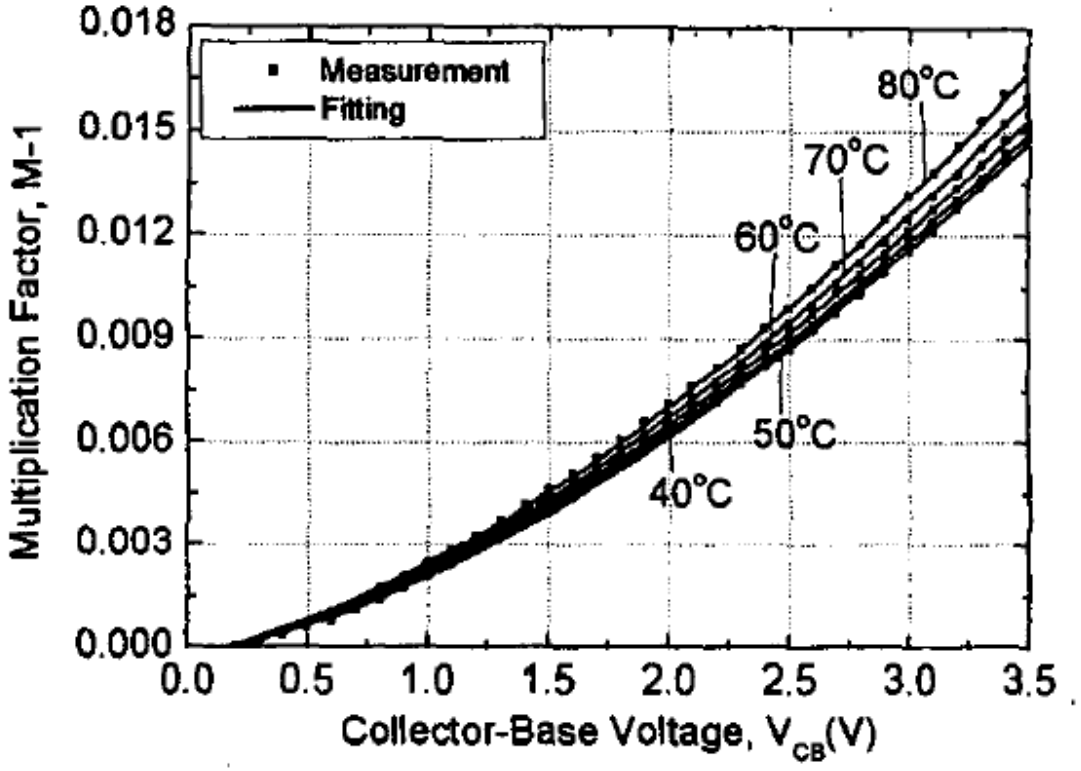


Figure 3.6: Large-signal equivalent circuit model of the InP/InGaAs SHBT [45].

The graph shown in Figure 3.6 along with equations 3.1 and 3.2 were used to determine the values of the empirical terms such that they fit the graph. The determined values are as follows:

$a_0(T_j)$ = -0.000428125

$a_1(T_j)$ = 0.00184375

$a_2(T_j)$ = 0.0006125

$a_3(T_j)$ = 0.000025

These values are then used to model the effects of self-heating and impact ionization in all simulations of the transistor as observed in Figure 3.4.

Thus the effects of self-heating and impact ionization effects were included for accurately modelling the breakdown behaviour. The noise model that was used includes thermal noise sources and shot noise. Flicker noise was neglected, as it is significant only at very low frequencies and therefore inconsequential in analogue transimpedance amplifier applications.

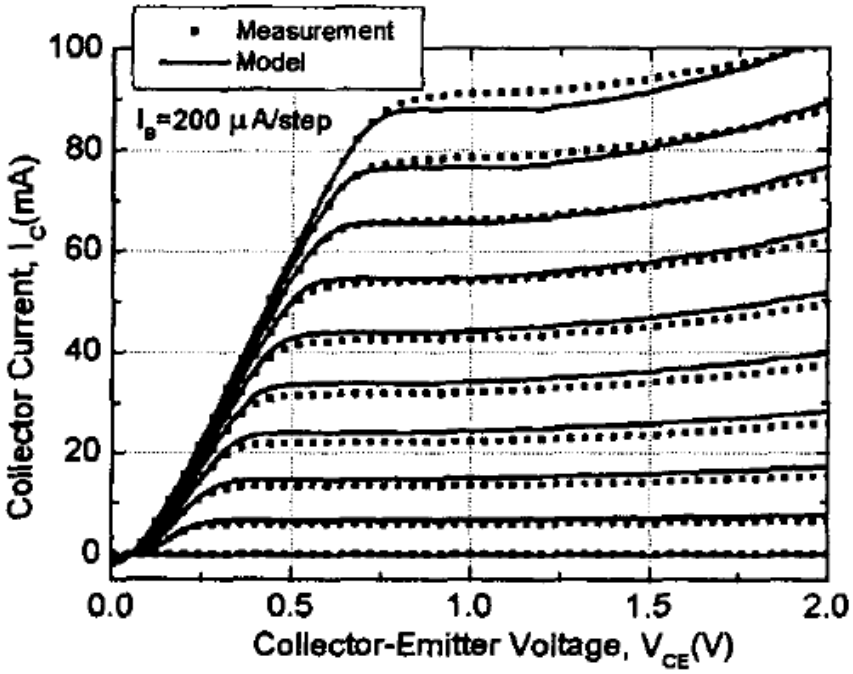
3.3.2 Calibration against Measured Results

In order to verify that the simulation of the transistor in ADS is correctly set up, the transistor was calibrated against both DC and AC measured results.

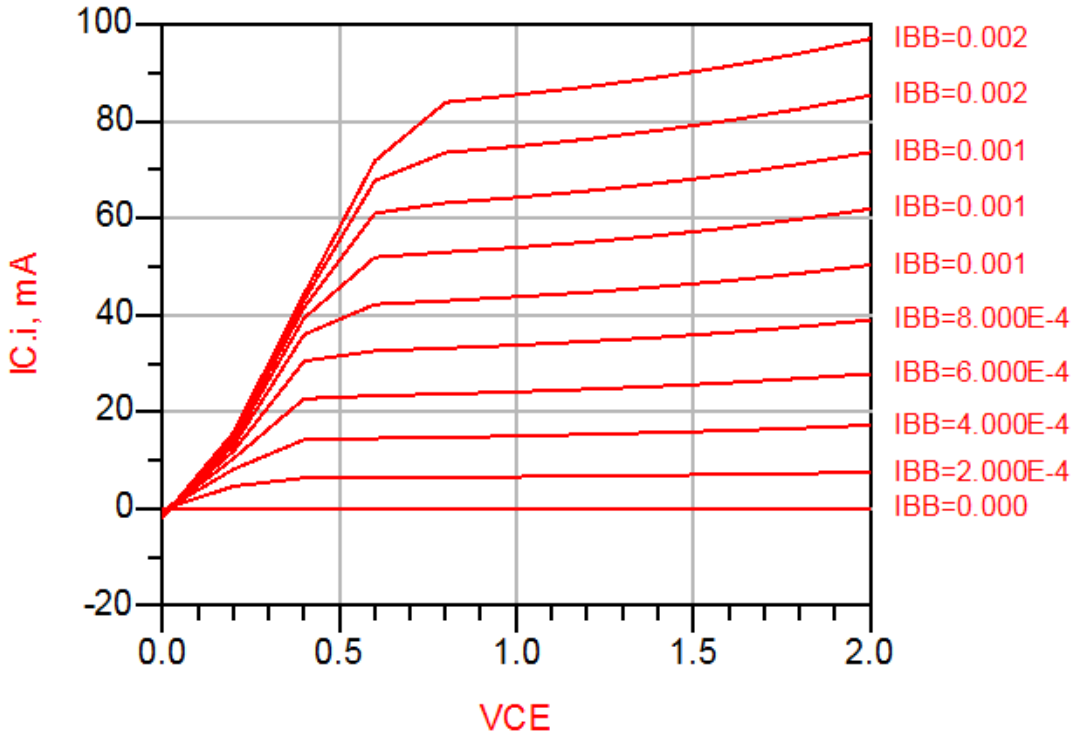
3.3.2.1 DC Calibration

For DC calibration, the IC-VCE characteristics under constant IB of the transistor were first produced through ADS simulation, and the simulated results were compared against the same characteristics of the transistor acquired through measured results, which were published in Figure 4 of [45]. The comparison results are shown in Figure 3.7.

As can be observed from Figure 3.7, the simulated results closely match the measured results, indicating that the simulation setup of the transistor is DC calibrated.



(a)



(b)

Figure 3.7: (a) Measured and modelled I_C-V_{CE} characteristics under a constant I_B bias condition reported in [45]. (b) I_C-V_{CE} characteristics under a constant I_B bias condition produced through ADS simulation in this work.

3.3.2.2 AC Calibration

For AC calibration, the S-parameters of the transistor between 0.5 GHz and 20 GHz at two different bias points (at IB=1.0mA; VCE=1.25V and IB=1.8mA; VCE=1.0V

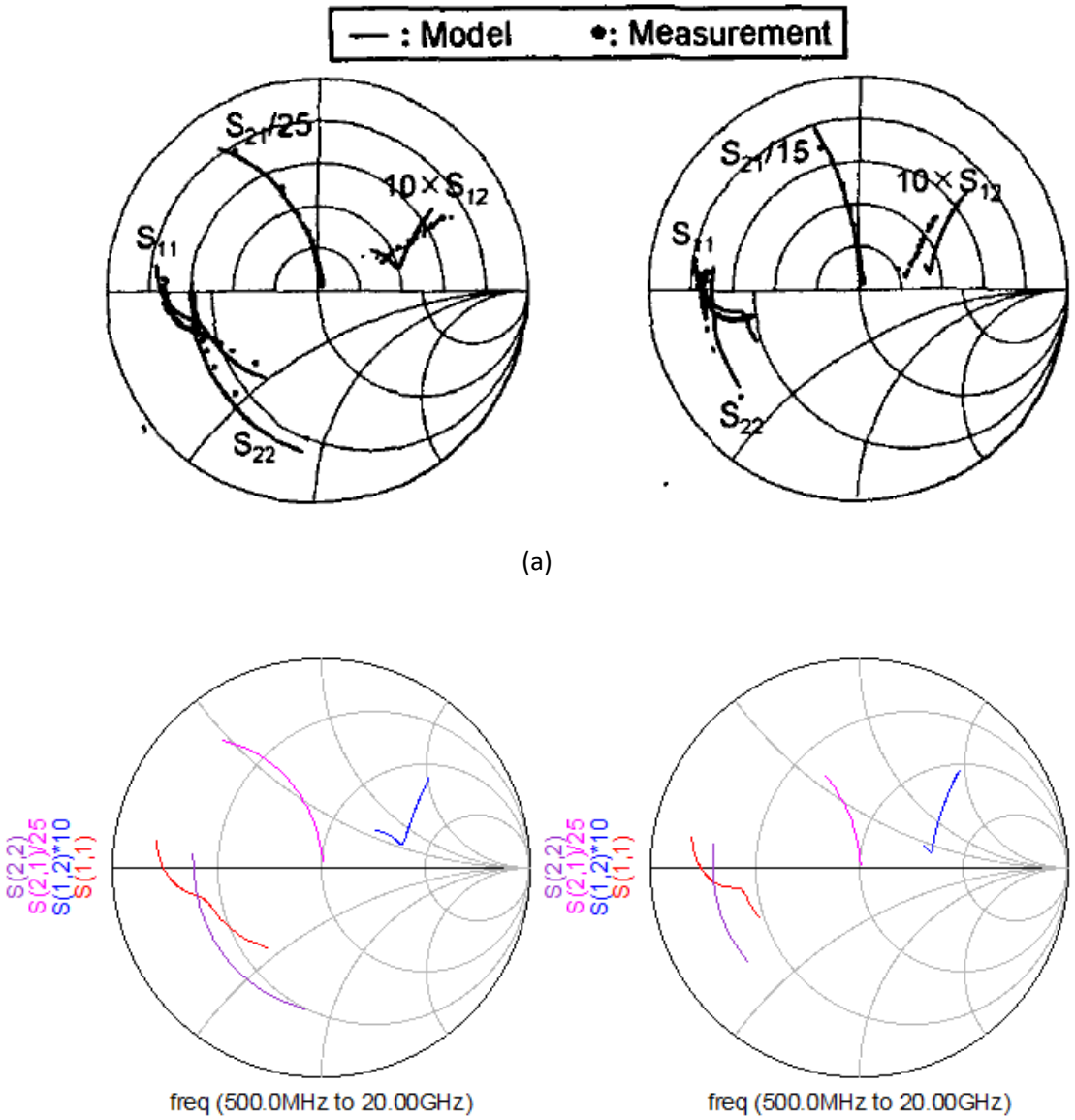


Figure 3.8: (a) Measured and modelled S-parameters from 0.5 GHz to 20 GHz for bias operating conditions of {I_B=1.0mA, V_{CE}=1.25V} (left) and {I_B=1.8mA, V_{CE}=1.0V} (right) as reported in [45]. (b) S-parameters from 0.5 GHz to 20 GHz for bias operating conditions of {I_B=1.0mA, V_{CE}=1.25V} (left) and {I_B=1.8mA, V_{CE}=1.0V} (right) produced through ADS simulation in this work.

respectively) are acquired though ADS simulation, and are then compared against measured S parameters of the transistor, which were published in Figure 6 of [45]. The comparison results are shown in Figure 3.8.

As can be observed from Figure 3.8, the simulated results are once again a very close match with the measured results, indicating that the simulation setup of the transistor is AC calibrated.

3.3.3 Other Considerations

The f_T of the transistor model that was used is about 63 GHz as long as the collector current I_c is biased between 15 mA and 25 mA. All of the transistors in each of the topologies were biased to meet this condition. The three amplifiers were simulated at an ambient temperature of 16.8 degrees Celsius.

Each of the transimpedance amplifiers was optimised to produce the best possible flat gain characteristics over a bandwidth of 25 GHz. The amplifier bandwidth was held as a constant for all three designs.

3.4 RESULTS

The three amplifiers were simulated using the Agilent Advanced Design System (ADS) simulation software [14]. The nonlinear harmonic balance simulator was used with the nonlinear noise mode activated. A two-tone test was performed on each amplifier, with harmonics of the input signals computed up to the fourth order. The maximum mixing order used in the simulations was three. The input current source was swept from 10 nA to 10 mA (–160 dB-Amps to –40 dB-Amps respectively). The

gain, gain-bandwidth product, output 1 dB compression point, spurious-free dynamic range (SFDR) and output noise power of the three preamplifiers were calculated. A 10 MHz noise bandwidth was used in the output noise power simulations. The results obtained are given in Table 3.1. Comparison of the transimpedance gain characteristics of the three amplifiers is shown in Figure 3.9.

The shunt-series amplifier has the best noise performance, even considering the effect of the slightly higher gain of the common-base input amplifier. It also has the best SFDR performance but this is offset by having the poorest gain-bandwidth product, output 1 dB compression point and transimpedance gain. The output power as a function of the input current is plotted in Figure 3.10(a) for the first harmonic and the

TABLE 3.1
SIMULATED TRANSIMPEDANCE AMPLIFIER
PERFORMANCE AT 10 GHZ (NOISE BANDWIDTH = 10 MHZ)

Parameter	Shunt-series	Common-base input	Distributed
Gain	29.3 dBΩ	31.0 dBΩ	39.9 dBΩ
Gain-bandwidth product	733.6 Ω-GHz	887.4 Ω-GHz	2473.9 Ω-GHz
Output 1dB compression point	-10.2 dBm	-2.5 dBm	+2.6 dBm
Output noise power	-101.2 dBm	-98.3 dBm	-84.1 dBm
Compressive dynamic range	91.0 dB	95.8 dB	86.7 dB
Spurious-free dynamic range	70.8 dB	70.2 dB	68.0 dB

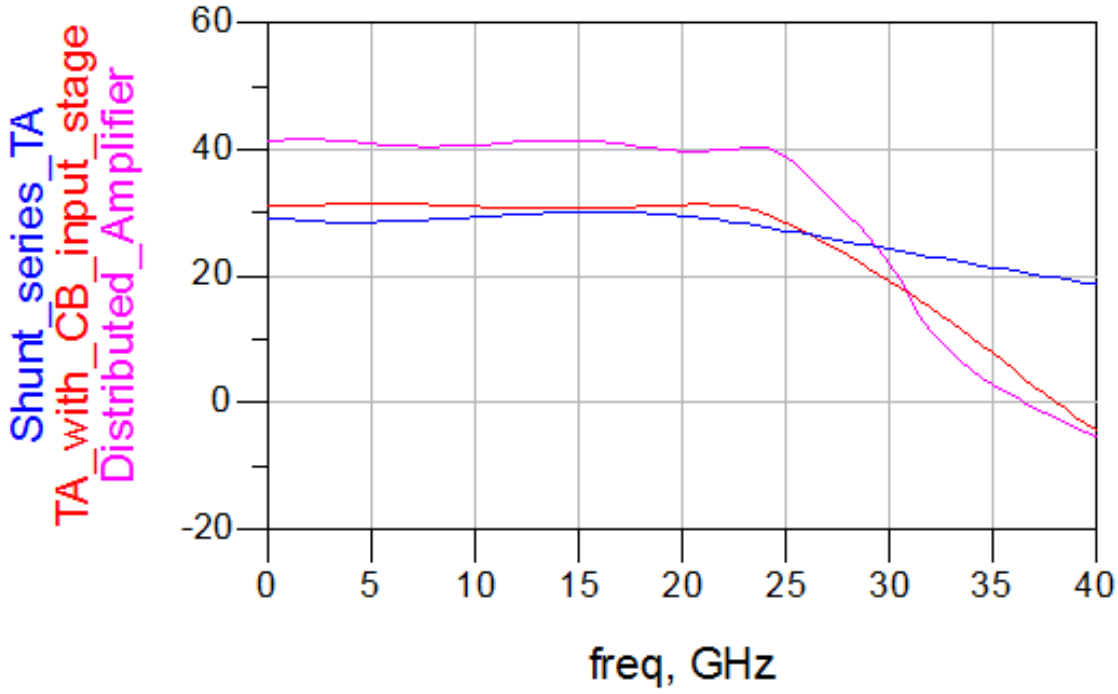


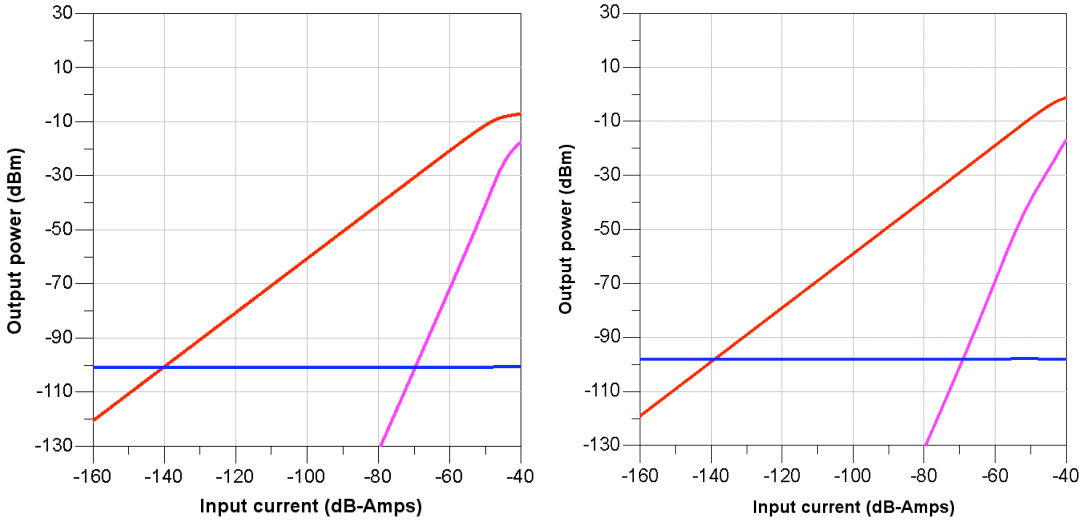
Figure 3.9: Gain characteristics of the three topologies.

IM3 intermodulation products. The early onset of gain compression at an input current of –48.5 dB-Amps is clearly evident.

The common-base input design shows an improvement in gain and gain-bandwidth performance over the shunt-series design. The noise performance is slightly degraded but is offset by a 7.7 dB improvement in the output 1 dB compression point. The compressive dynamic range (CDR) of 95.8 dB is clearly the best of the three amplifiers considered. The SFDR performance is also very good and only 0.6 dB below that of the shunt-series configuration. The output power as a function of the input current is plotted in Figure 3.10(b).

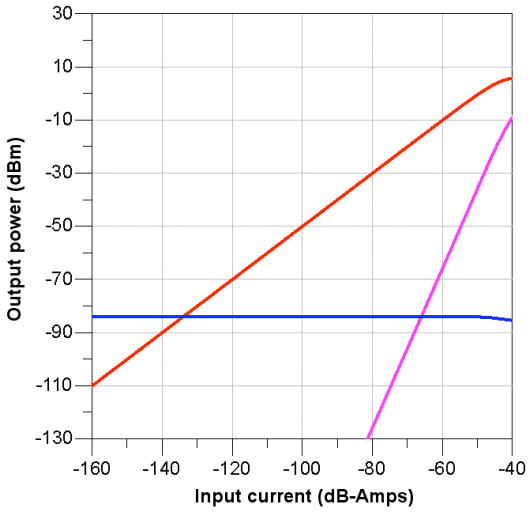
The distributed amplifier, although slightly inferior in terms of CDR and SFDR, is superior to the other two designs by far in terms of gain, gain-bandwidth product, and output 1dB compression point. The gain-bandwidth product is approximately 2.8

times that of the common-base input amplifier (consistent with the 8.9 dB improvement in transimpedance gain). The output characteristics versus input current are shown in Figure 3.10(c).



(a)

(b)



(c)

Figure 3.10: The output power as a function of input current for the first harmonic and IM3 products of the (a) shunt-series, (b) common-base input and (c) distributed transimpedance amplifiers at 10 GHz. The noise floor is also presented (calculated for a 10 MHz noise bandwidth).

The increase in the output noise power is clearly evident and cannot be solely attributed to the increased gain of the amplifier. It clearly indicates that the distributed amplifier has a poorer noise figure than the common-base input design.

3.5 SUMMARY OF FINDINGS AND CONCLUSION

A comparison of the dynamic range performance of three representative InP HBT transimpedance amplifier topologies has been presented. The feedback amplifier topologies were found to yield the best noise performance with the common base input topology providing a CDR of 95.8 dB and a SFDR of 70.2 dB. The distributed amplifier topology, however, produced a gain-bandwidth product 2.8 times that of the common-base input topology and yielded a SFDR of 68.0 dB. The considerably greater gain-bandwidth product suggests that the distributed amplifier is capable of considerably wider bandwidths than the feedback topologies while maintaining comparable SFDR performance.

Even though SFDR performance of the transimpedance amplifier is one of the main focuses of the project and the distributed amplifier was found to have the worst SFDR performance, it was still comparable with the SFDR performance of the other topologies. On the other hand, the distributed amplifier topology excels over the other options by far in terms of gain and bandwidth performance, which are also important figures of merit in this work. The significant strength of the distributed amplifier topology in terms of gain and BW over the other options is considered to more than make up for its slight weakness in terms of SFDR As such, **the distributed amplifier topology is selected for use in this work**.

As already mentioned previously, the aforementioned findings were peer reviewed and accepted for presentation at the Asia Pacific Microwave Conference 2009 and were later published in the corresponding conference proceeding [106].

Chapter Four:

Circuit Design Techniques for SFDR Improvement

4.1 INTRODUCTION

It was established in the last chapter that the distributed amplifier topology is significantly superior compared to other design topologies for HBT transimpedance amplifiers in terms of gain bandwidth product while retaining a comparable SFDR performance. The distributed amplifier topology will become even better suited for HBT transimpedance amplifiers for OEIC analogue applications, if its SFDR (which

was its only weakness when compared with other options) can be further improved. This chapter therefore will focus on tradeoff options for the achievement of high SFDR in HBT transimpedance distributed amplifiers. We will introduce and analyse three different techniques to improve the SFDR of HBT transimpedance amplifiers at the expense of their transimpedance gain performance. These techniques are meant to provide designers with the flexibility to predict and improve SFDR by sacrificing the transimpedance gain, in applications where SDFR is the highest priority. Each of the techniques will be theoretically analysed and then illustrated by a design example and the analytically predicted response will be compared with the results obtained by computer-aided circuit analysis. All three of these techniques were devised by the author as novel techniques as will be elaborated in much more detail in section 4.3, and they led to a peer reviewed journal publication titled "*An investigation of tradeoff options for the improvement of spurious-free dynamic range in HBT transimpedance distributed amplifiers*" in the PIER L (Progress in Electromagnetic Research Letters) journal (http://www.jpier.org/PIER/) in 2012.

4.2 REFERENCE DESIGN

As a starting point for each of our design examples, we will use an HBT transimpedance distributed amplifier designed using a methodology described and used by Cohen *et al.* [25], which is based on and improves a methodology proposed by Kobayashi *et al.* [50]. This methodology has also been used by Kraus *et al.* [12] to design an HBT transimpedance amplifier with excellent performance as recently as 2007. In that work, a HBT transimpedance distributed amplifier bandwidth of

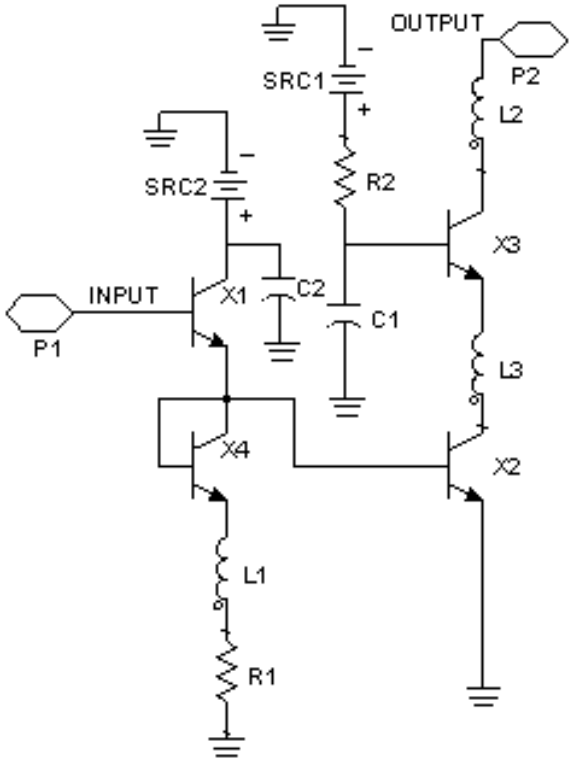


Figure 4.1: Schematic of a single gain stage of the Reference design by Cohen[25].

54.2 GHz at a transimpedance gain of 170 Ω, i.e. 44.61 dBΩ, was achieved using HBT transistors with an f_T value of only 70 GHz. The linearity performance of this amplifier was not reported as amplifier linearity was not a priority in that work, and therefore the achieved linearity performance is not known. To the best of the author's knowledge, this is the best performance in terms of gain-bandwidth product and bandwidth efficiency for a HBT transimpedance distributed amplifier reported till date. Therefore this methodology for HBT transimpedance amplifier design was regarded as the state of the art. The topology that Cohen uses for each gain stage or gain cell comprises an emitter follower at the input followed by a cascode, as shown in Figure 4.1. An overview of this topology along with functional details each of the aforementioned parts of the gain stage is discussed in more detail in section 3.2.3. For

the design, we used InP/InGaAs HBTs in our transimpedance distributed amplifier, in accordance with selections of transistor type and semiconductor materials made in chapter 2. The parameters of the HBT transistor model that we used in the amplifier were taken from [45], which reports experimentally verified large signal model parameters of an actual InP/InGaAs HBT. This amplifier design will be regarded as the reference design for the work described in this chapter. This reference design will be used as a starting point for the design examples demonstrating each of the techniques that are being proposed to improve the SFDR, and the performance of each of the techniques will be measured against the performance of this reference design.

Following this reference design methodology for the design of the gain stages and using Beyer's design methodology [95] for the distributed amplifier design, the optimal number of gain stages for the amplifier was calculated to be 4, and the reference amplifier was designed and simulated to have a relatively flat transimpedance gain of about 43.3 dBΩ at up to 30 GHz and a large signal SFDR of about 66.3 dB, as shown in Figure 4.2. A noise bandwidth of 10MHz has been used for this and all other SFDR simulations in this work.

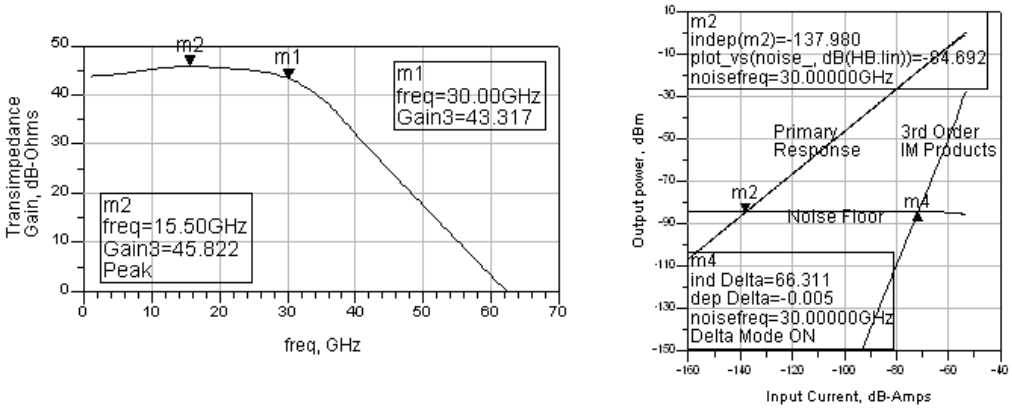


Figure 4.2: Transimpedance gain vs. frequency characteristics and the large signal SFDR produced by the reference design (Cohen [25]) at 30 GHz.

4.3 SFDR ENHANCEMENT TECHNIQUES WITH DESIGN EXAMPLES

4.3.1 Technique 1: Replacement of Emitter follower Section

The emitter follower section preceding the cascode section in the gain stage shown in Figure 4.1 was originally proposed by Kobayashi *et al.* [50] and was intended to transform the capacitive impedance at the input of the cascode section to generate negative resistance at the input of the gain stage in order to achieve attenuation compensation on the input line. The objective was to improve the gain bandwidth product of the DA. However, as the emitter follower also performs current amplification, it has a detrimental effect on the linearity of the DA. In order to verify this, we performed a two-tone spectral analysis on each of the four gain stages of the standard amplifier. The results of this analysis carried out at 30(±0.05) GHz and an arbitrary input current of 2.2 mA is shown in Figure 4.3, which shows the voltage level at the input of each gain stage denoted by the blue arrows, the voltage level between the emitter follower section and the cascode section (i.e. the voltage level at the output of the emitter follower section and the input of the cascode section) of each gain stage denoted by the violet arrows and the voltage level at the output of each gain stage denoted by the red arrows. For each gain stage, these voltage levels are shown for both the primary tones and the third-order intermodulation products. As can be observed from the figure, for each of the four gain stages, the emitter follower amplifies the third order intermodulation products and at the same time attenuates the primary tones, while only the cascode section amplifies the primary tones. Although

Figure 4.3 only shows results for 30(±0.05) GHz and an arbitrary input current level of 2.2 mA, the analysis was also carried out for a number of other input current levels and for 10(±0.05) GHz and 20(±0.05) GHz, with very similar results and observations in each case. Thus from this analysis, we learned that the emitter follower section

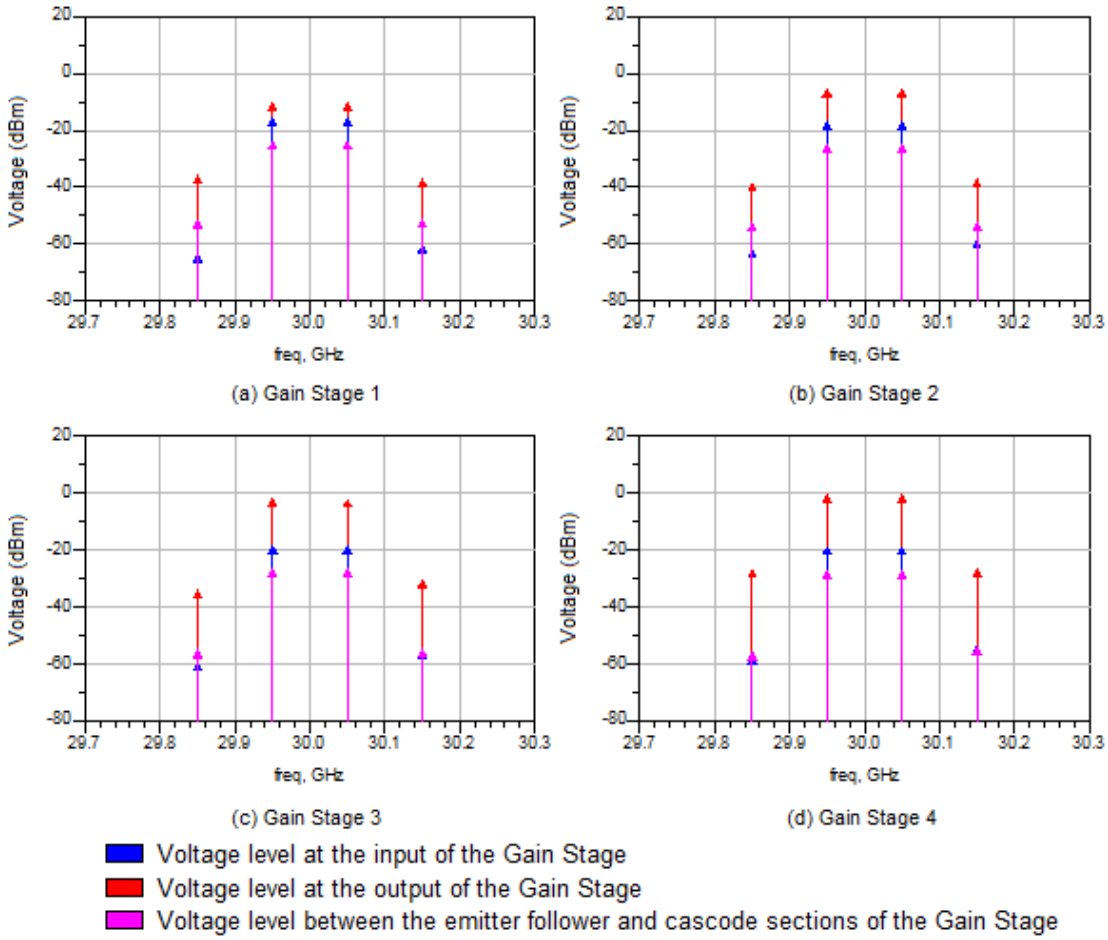


Figure 4.3: Two-tone spectral analysis on each of the four gain stages of the standard amplifier showing the effect of the emitter follower section on the linearity of the amplifier at 30(±0.05) GHz and an amplifier input current of 2.2 mA.

attenuates the primary response, but it increases the third order products, thereby degrading the SFDR performance. As linearity and dynamic range are the priority in this work, we decided to remove the emitter follower section in order to negate the nonlinearities caused by this section as discussed above, and introduce a parallel RC section in its place in order to increase the input impedance of the gain stage, as

shown in Figure 4.4. The purpose of the capacitor in the parallel RC section is to reduce the input capacitance of the gain stage, while the resistor is used for biasing. We verified the results of this replacement by repeating the two-tone spectral analysis on each of the four gain stages of the altered amplifier. The results of this analysis at 30(±0.05) GHz and an input current of 2.2 mA is shown in Figure 4.5, which shows

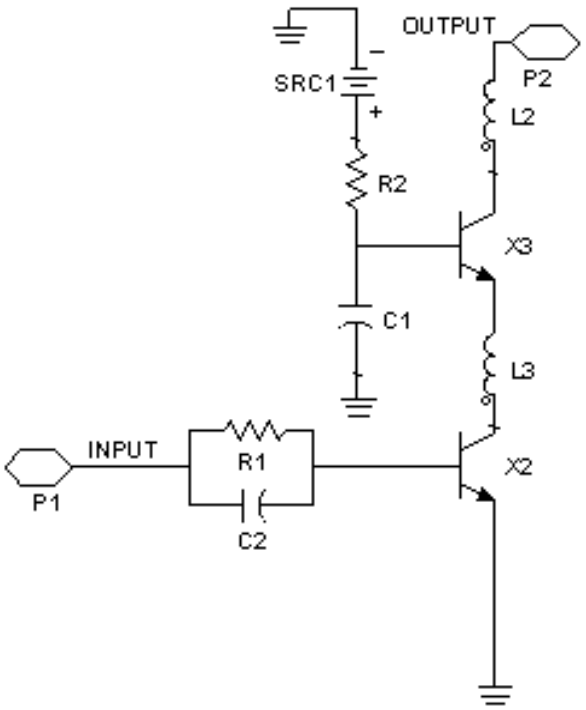


Figure 4.4: Schematic of a single gain stage of the altered design with the emitter follower section replaced by a parallel RC section.

the voltage level at the input of each gain stage denoted by the blue arrows, the voltage level between the parallel RC section and the cascode section (i.e. the voltage level at the output of the parallel RC section and the input of the cascode section) of each gain stage denoted by the violet arrows and the voltage level at the output of each gain stage denoted by the red arrows. Once again, for each gain stage, these voltage levels are shown for both the primary tones and the third-order

intermodulation products. As can be observed from the figure, for each of the four gain stages, as a result of the replacement of the emitter follower section with the parallel RC section, the third order intermodulation products are no longer amplified by the first section, i.e. the parallel RC section, while the primary tones are only slightly attenuated by it. Once again, the analysis was repeated for a number of other input current levels and for 10(±0.05) GHz and 20(±0.05) GHz, with very similar results and observations in each case. Thus it was verified that in this case, the input capacitor (relatively slightly) attenuates the primary response, but does not generate additional third order products which results in better linearity. However, it was understood that this removal of the emitter follower section would naturally result in a drop in gain, because as previously discussed in section 3.2.3, the role of the emitter follower section was to achieve attenuation compensation of the input transmission line by transforming the capacitive impedance at the input of the cascode section to generate negative resistance at the input of the gain stage, which is no longer achieved upon its removal and replacement. Accordingly, the linearity and SFDR is improved with this replacement over that obtained with the emitter follower at the input of the gain stage, at the cost of a reduction in gain.

In order to make a fair comparison of performance with the reference design, the resistor in the parallel RC section was adjusted to retain the DC biasing in the cascode section, while the capacitor was adjusted to attain a flat input capacitance characteristic for the gain stage. We found that this resulted in the SFDR improving from 66.3 dB to 71.8 dB at 30 GHz which is a 5.5 dB improvement. The gain dropped from 43.3 dBΩ to 34.5 dBΩ, which is an 8.8 dB gain tradeoff, as shown in Figure 4.6 and presented along with results for other frequencies (10 and 20 GHz) in Table 4.1.

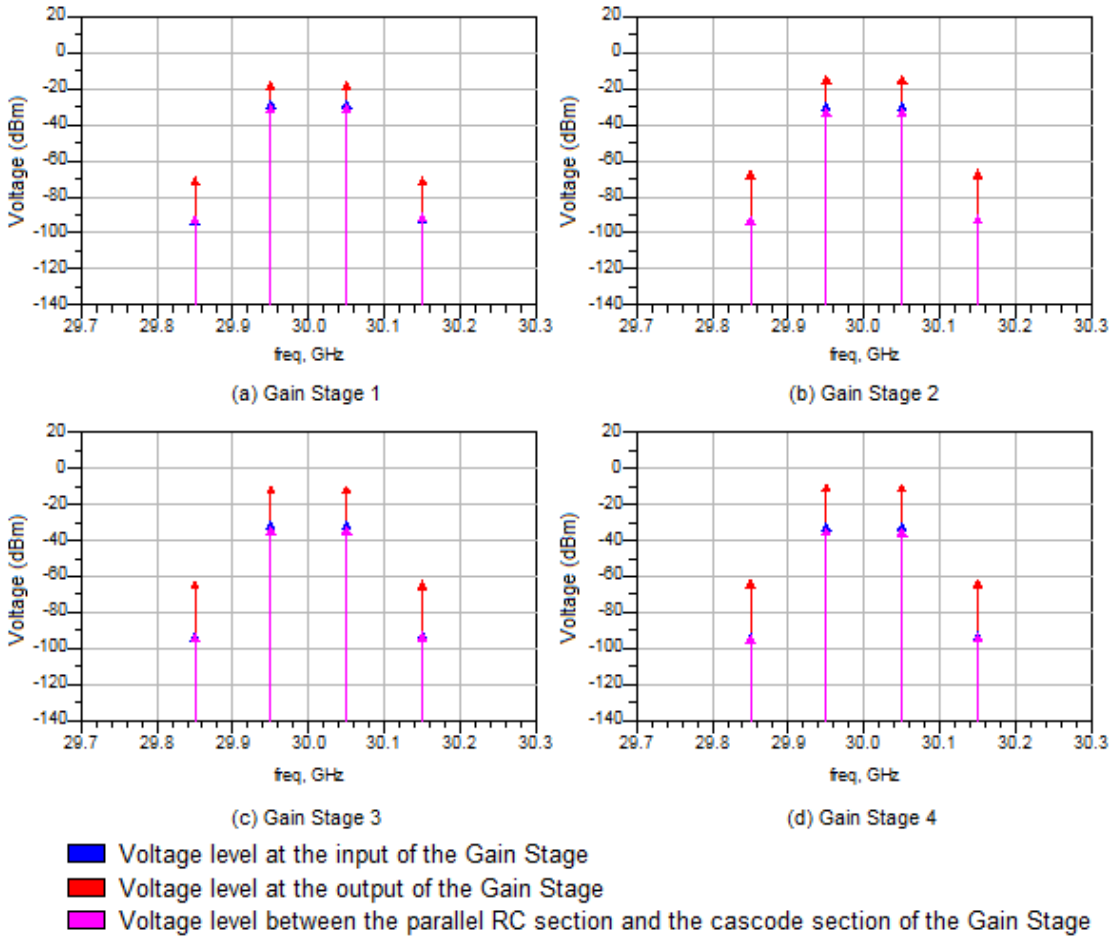


Figure 4.5: Two-tone spectral analysis on each of the four gain stages of the altered amplifier showing the effect of the replacement of the emitter follower section with the parallel RC section on the linearity of the amplifier at 30(±0.05) GHz and an amplifier input current of 2.2 mA.

A comparison of the noise floor level of the amplifier with the emitter follower section (the reference design) and the amplifier with the parallel RC section was also made. It was found that the noise floor was about 5 dB lower with the parallel RC section. This drop is less than the 8.8 dB reduction in gain, so the introduction of the parallel RC section has degraded the amplifier noise figure. Nonetheless, an overall improvement in SFDR is still obtained.

Although this technique was devised by the author as a novel technique for this work, the author later discovered that variations of this technique have been used by

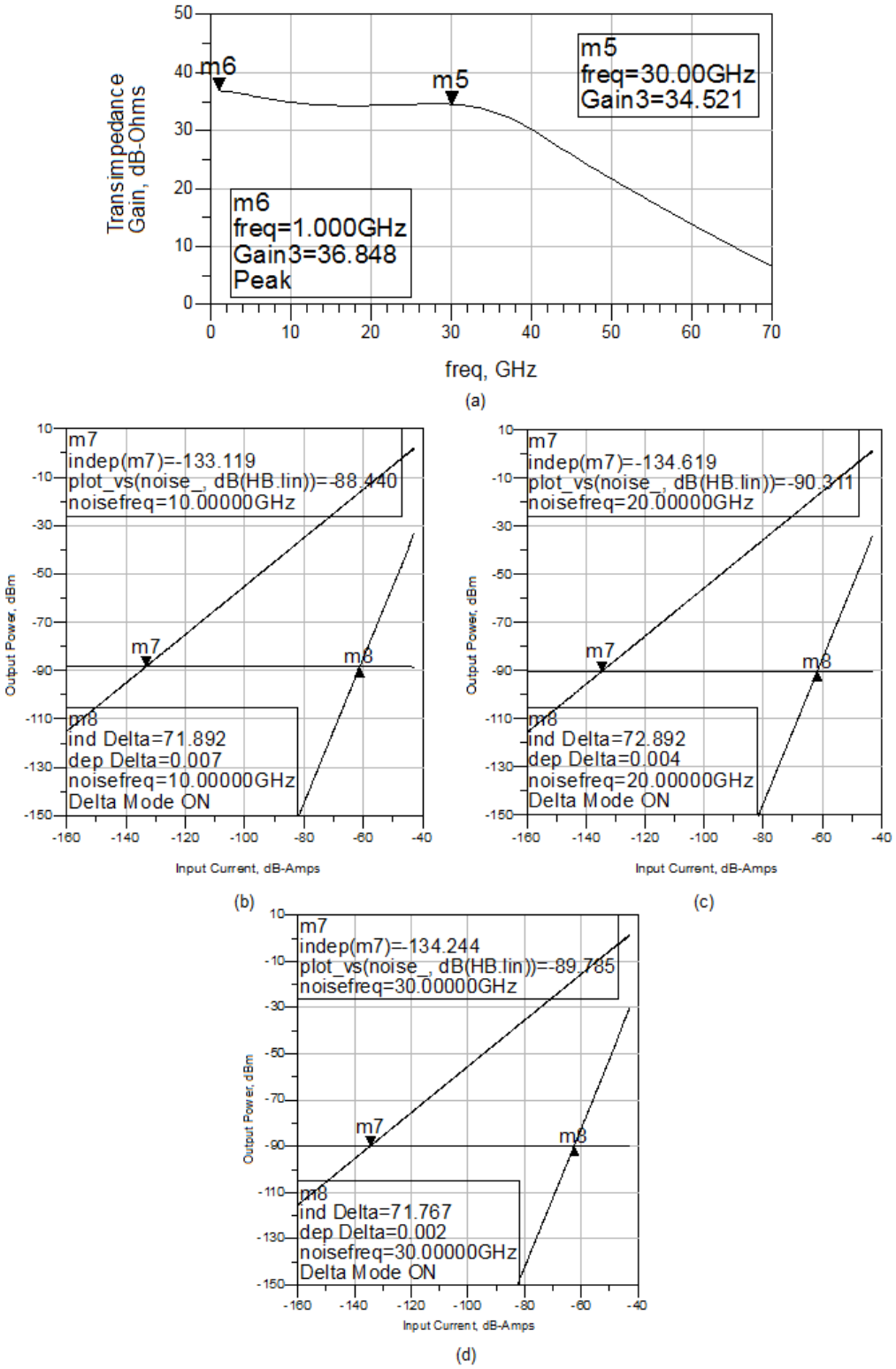


Figure 4.6: Results for Technique 1 design example:
(a) Changed Transimpedance gain vs. frequency characteristics
(b) Large signal SFDR produced by the Technique 1 design example at 10 GHz
(c) Large signal SFDR produced by the Technique 1 design example at 20 GHz
(d) Large signal SFDR produced by the Technique 1 design example at 30 GHz

designers in past work in order to attain linearity [51]. However its details and performance have not been adequately researched to the best of the author's knowledge. This work discusses it in detail and compares its performance with other techniques that are introduced in this work.

4.3.2 Technique 2: Adjustment of Amplifier Load

Most of the load power generated by a distributed amplifier is contributed by the last few stages nearest the load, and almost half the total output power is generated by the stage nearest the load [52]. According to equation (15) of [52], the output voltage across the k^{th} gain stage of an n stage distributed amplifier is given by

$$V_{ds,k} = \frac{Z_\pi}{2} g_m V_{gs,1} e^{-j(k-1)\theta} \left\{ k + \frac{e^{-j2\theta} - e^{-j2(n-k+1)\theta}}{1 - e^{-j2\theta}} \right\} \tag{4.1}$$

where g_m is the transconductance of each gain stage, $V_{gs,1}$ is the input voltage of the first gain stage, i.e. the gain stage that is furthest from the load, Z_π is the image impedance of the Pi sections of the input and output transmission lines and θ is the electrical length between two adjacent gain stages, i.e. the propagation constant of each of the Pi sections of the input and output transmission lines. These terms are defined and explained in more detail in [52].

According to equation (13) of [52], the current injected by the k^{th} stage of the amplifier into the output line is given by

$$I_k = g_m V_{gs,1} e^{-j(k-1)\theta} \tag{4.2}$$

If we let $\omega << \omega_c$, (where ω_c is the 3 dB cutoff frequency of both the input and

output transmission lines) then $Z_\pi \cong Z_0$ where Z_0 is the characteristic impedance of the output line and the load impedance of the amplifier. Therefore the load seen by the k^{th} gain stage can be calculated as follows using the previous two equations.

$$Z_{L,k} = \frac{V_{ds,k}}{I_k} = \frac{Z_0}{2}\left\{k + \frac{e^{-j2\theta} - e^{-j2(n-k+1)\theta}}{1 - e^{-j2\theta}}\right\} \tag{4.3}$$

Therefore the load seen by the last stage (*i.e.* with $k = n$),

$$Z_{L,n} = \frac{Z_0 n}{2} \tag{4.4}$$

Taking the effect of the output line capacitance, C_{ds} on $Z_{L,k}$ into account, we get,

$$Z_{L,n} = \frac{Z_0 n}{2 - j2\pi f C_{ds} Z_0 n} \tag{4.5}$$

Equation (4.5) shows that the load seen by the final stage is a function of the load of the amplifier, and therefore the load seen by the final stage can be adjusted to a certain degree by adjusting the load of the amplifier.

Running a load-pull analysis simulation on the last gain stage of the amplifier generates 3rd order IMD (intermodulation distortion) contours on the Smith chart, which allows us to predict the 3rd order IMD and therefore the linearity performance of the gain stage for any given $Z_{L,n}$ value. As almost half the output power is generated by the last stage over most of the frequency range [52], it can be assumed most of the nonlinearity is also generated by the last stage. Therefore the nonlinearity of the amplifier can be adjusted by varying $Z_{L,n}$, which can be done by tuning the load of the amplifier, Z_0 as Equation (4.5) suggests. Thus the value of Z_0 can be adjusted or

tuned to improve the dynamic range of the amplifier. However, changing Z_0 will also have an effect on the gain of the amplifier, and in most cases, changing Z_0 to improve the SFDR will have a negative effect on the transimpedance gain, which is the tradeoff.

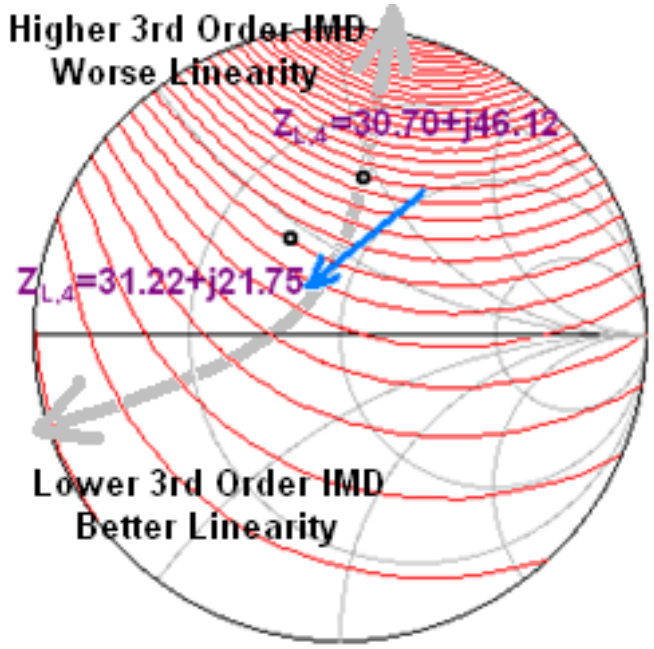


Figure 4.7: Third order IMD contours generated from load-pull simulation of a single gain stage of the reference design, at 30 GHz and at an input power level of -25 dBm. $Z_{L,4}$ values for Z_0 = 50 Ω and Z_0 = 23.19 Ω are shown. The contour step size is 1 dB.

Third order IMD contours generated by Agilent ADS software [14] from load-pull simulation of a single gain stage of the reference design at 30 GHz and at an input power level of -25 dBm (which is an arbitrary input power level for which the 3rd order intermodulation is higher than the noise floor but lower than the 1 dB compression point) are shown in Figure 4.7. From Equation (4.5), we can calculate that for a 50 Ω amplifier load (Z_0), the load seen by the final stage of the amplifier, i.e. the fourth stage of the amplifier, $Z_{L,4}$ = 30.70 + j46.12 Ω (notably the values of both *n*

and C_{ds} are known for this calculation as they have been determined using Beyer's methodology [95] during the initial design of the reference amplifier mentioned in section 4.2). Once we plot this calculated $Z_{L,4}$ value, i.e. 30.70 + j46.12 Ω, on the Smith chart as shown in Figure 4.7, we are in a position to predict whether the linearity of the amplifier would improve or worsen from its current state for any changed Z_0 value, by using equation 4.5 to recalculate the corresponding $Z_{L,4}$ value for the changed Z_0 value, plotting the recalculated $Z_{L,4}$ value on the Smith chart with the third order IMD contours shown in Figure 4.7 in order to determine which direction the newly plotted $Z_{L,4}$ has moved in the Smith chart from its original position and lastly using the contours shown in Figure 4.7 to determine whether the changed Z_0 value would result in better or worse linearity. Thus Z_0 can be tuned at the discretion of the designer to reach a point in the Smith chart in Figure 4.7 where the linearity is improved. As an example, tuning the amplifier load Z_0 from 50 Ω to an arbitrary value 23.19 Ω and re-adjusting (in accordance with Beyer's distributed amplifier design principles [95]) all elements of the distributed amplifier circuit (such as the output line inductance L_d, input line inductance L_g, the input line termination, Z_{0g}, etc.) results in the value of $Z_{L,4}$ to change from 30.70 + j46.12 Ω to 31.22 + j21.75 Ω according to Equation (4.5). As we can see from Figure 4, this causes $Z_{L,4}$ to move to a location on the Smith chart where the 3rd order IMD of the final gain block is lower and therefore the linearity is better. Finally, the output of the amplifier is matched to a 50 Ω load using an impedance matching network. Any wideband impedance matching network type can be used for the impedance matching, keeping in mind that distributed amplifiers generally have very high bandwidth. For this example, we used a tapered line transformer network for the impedance matching by designing it to

match the amplifier Z_0 of 23.19 Ω to a 50 Ω load across the bandwidth of the amplifier, i.e. 30 Ghz, the schematic design of which is shown in Figure 4.8.

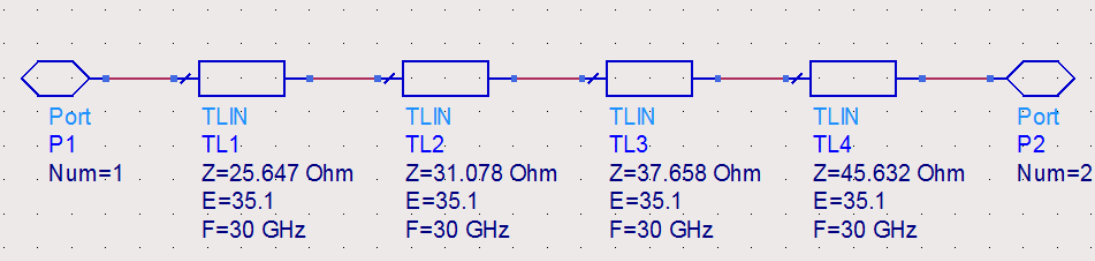


Figure 4.8: Schematic design of the tapered line transformer network used for wideband impedance matching of the amplifier Z_0 of 23.19 Ω to a 50 Ω load across the bandwidth of the amplifier, i.e. 30 Ghz.

Thus we can use Equation (4.5) and load pull analysis of the gain block to analytically predict that decreasing Z_0 will result in better linearity. Understandably, this procedure of using a lower Z_0 value will result in a lower transimpedance gain. Thus lower 3rd order IMD, i.e. better linearity and better SFDR, can be achieved by trading off transimpedance gain. The exact amount by which to reduce Z_0 will depend on the gain and SFDR requirements of the specific case and the discretion of the designer. However, reducing it too much will not only drastically reduce gain, but also make it difficult to match the output to 50 Ω.

For our example, reducing Z_0 from 50 Ω to 23.19 Ω and then making necessary adjustments to the appropriate circuit elements as per the reference design methodology and using an impedance matching network to match the 23.19 Ω output to a 50 Ω load resulted in the SFDR to move up from 66.3 dB to 70.3 dB at 30 GHz, which is a 4 dB improvement. However, the gain dropped from 43.3 dBΩ to 34.5 dBΩ, which is an 8.8 dB gain tradeoff. The results are shown in detail in Figure 4.6 and summarized in Table 4.1.

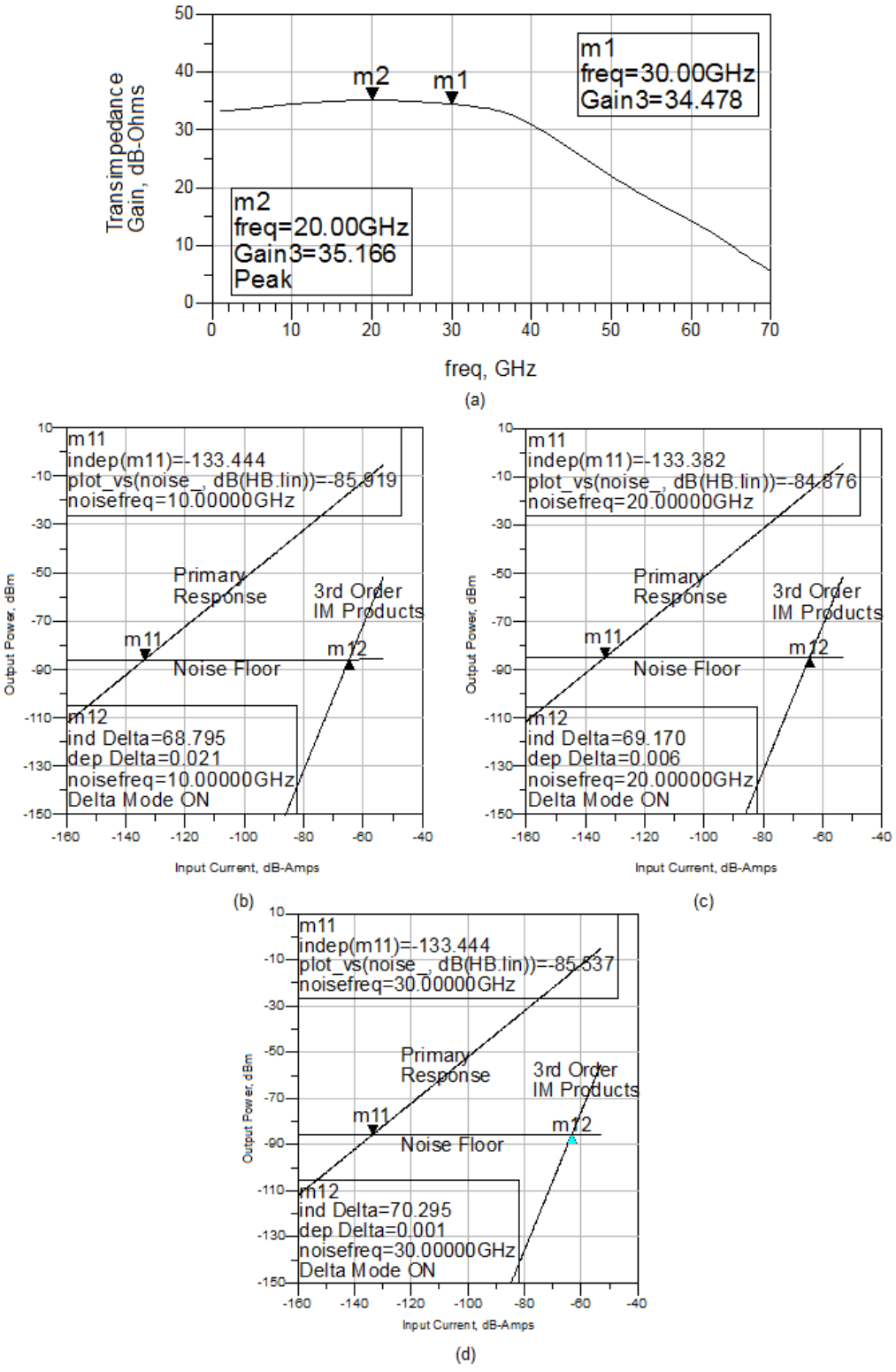


Figure 4.9: Results for Technique 2 design example:
(a) Changed Transimpedance gain vs. frequency characteristics
(b) Large signal SFDR produced by the Technique 2 design example at 10 GHz
(c) Large signal SFDR produced by the Technique 2 design example at 20 GHz
(d) Large signal SFDR produced by the Technique 2 design example at 30 GHz

4.3.3 Technique 3: Adjustment of Cascode Base Capacitor

In an attempt to improve output power performance of HBT Distributed Amplifiers, Fraysse *et al.* in 2000 [53] added a capacitance C_a between the base of the common base HBT and ground, which allows the control of voltage across the input of the common base HBT by voltage division between C_a and C_{be} of the common base HBT. Therefore it also allows the control of the load that the common emitter HBT sees to a certain degree. Running a load-pull simulation on the common emitter HBT allows us to see how the linearity of the HBT varies with varying the load that it sees, which can then be optimized as necessary via optimization of the capacitance that is the equivalent of C_a in our design, which is denoted as C1 in Figure 4.1.

Load-pull analysis simulation is performed on the common emitter HBT in our gain stage (denoted as X2 in Figure 4.1) at 30 GHz in order to generate 3rd order IMD contours as shown in Figure 4.10. These contours indicate the load preferences for X2 for low 3rd order intermodulation distortion and better linearity. In order to study how the load impedance of X2 varies as the capacitor C1 is varied, we swept the C1 value. We found that decreasing C1 causes the load impedance to move towards lower 3rd order IMD positions, as indicated by the contours. This indicates that in this case, using a lower capacitor value for C1 will result in lower 3rd order IMD, i.e. better linearity and higher SFDR. However, a lower C1 value will have a negative effect on the gain of the amplifier, because it will cause a higher reactance at the base of the common base HBT which will result in a higher resistive element in the output impedance of the gain stage. Therefore the exact amount by which to reduce C1 will be a tradeoff between gain and SFDR. An additional downside of this technique is that the output impedance of the gain stage will be affected to different extents at

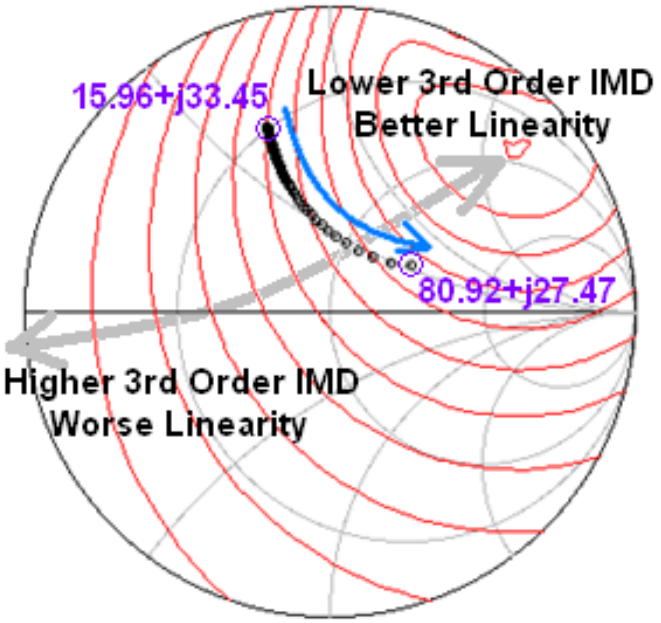


Figure 4.10: Third order IMD contours generated from load-pull simulation of the common emitter HBT transistor X2 (in Figure 4.1). Load impedances of X2 for C1 values ranging from 10 pF to 0.25 pF in steps of -0.05 pF are shown. The contour step size is 1 dB.

different frequencies, i.e. the output impedance at higher frequencies will be affected much more compared to that at lower frequencies as higher frequencies are more sensitive to the change of the capacitance value, which will result in more gain being traded off at higher frequencies compared to lower frequencies causing a compromise of flat gain characteristics of the amplifier. Thus, if the capacitor is tuned too much, maintaining a flat gain response of the amplifier becomes difficult for the designer.

For this example, reducing C1 from 10 pF to 0.25 pF in steps of -0.05 pF caused the load impedance of X2 to change from 15.96 + j33.45 Ω to 80.92 + j27.47 Ω. Figure 4.10 shows the load impedances of X2 at various C1 values, and the arrow indicates the direction that the load moves as C1 is reduced. As can be observed from Figure 4.10, this caused the load impedance of X2 to move to a lower 3rd order IMD position,

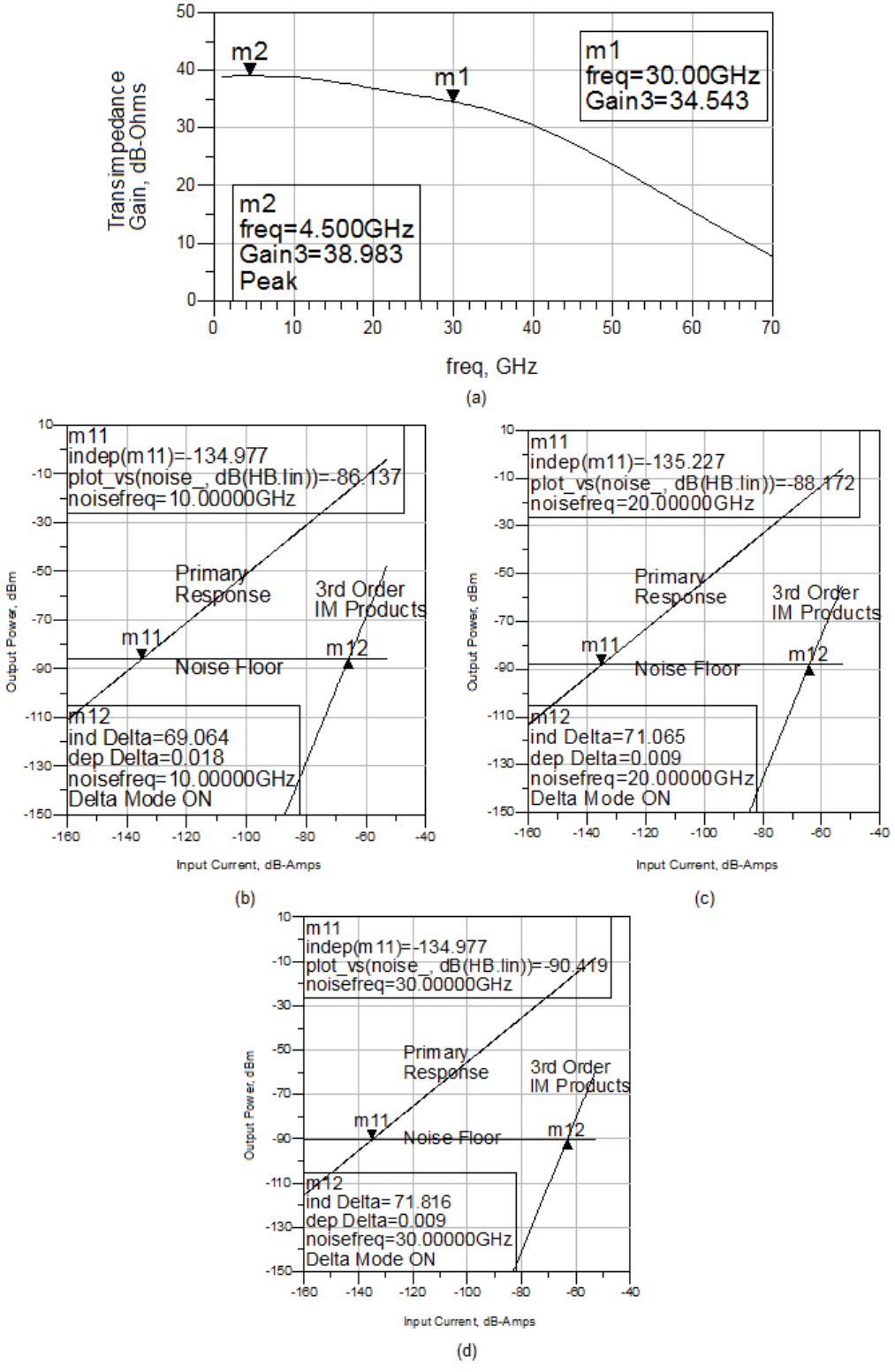


Figure 4.11: Results for Technique 3 design example:
(a) Changed Transimpedance gain vs. frequency characteristics
(b) Large signal SFDR produced by the Technique 3 design example at 10 GHz
(c) Large signal SFDR produced by the Technique 3 design example at 20 GHz
(d) Large signal SFDR produced by the Technique 3 design example at 30 GHz

which resulted in a 5.5 dB SFDR improvement (from 66.3 dB to 71.8 dB). However, the gain dropped from 43.3 dBΩ to 34.5 dBΩ as can be observed in Figure 4.11. As discussed earlier in the section, the flat gain characteristic of the amplifier is also sacrificed to a certain degree, which is also observed in Figure 4.11. Figure 4.11 also shows further details including improvements at other frequencies that are also presented in Table 4.1.

4.4 RESULTS AND OBSERVATIONS

Table 4.1 shows comparisons between the reference design and design examples of each of the techniques in terms of their gain and SFDR performances. In our design examples for each of the three techniques, an equal amount of gain was traded off (from 43.3 dBΩ to 34.5 dBΩ) at 30 GHz from the reference design on purpose, so that a fair comparison can be made between the three techniques in terms of SFDR improvement.

As can be observed from Table 4.1, Technique 2 produced the least SFDR improvement among the three. Techniques 1 and 3 on the other hand have performed similarly in terms of SFDR improvement. However each of these two techniques has its drawback. As Technique 1 is basically the replacement of the emitter follower section with a parallel R-C network followed by appropriate adjustments as detailed in section 4.3.1 (i.e. DC biasing of the gain stage, adjustment of the parallel capacitor value in order to attain gain flattening, etc.), this technique is not at all tunable in terms of tradeoff, and therefore significantly lacks flexibility. On the other hand, Technique 3, although fully tunable via the capacitor, compromises the flat gain

response of the amplifier to an extent as discussed in section 4.3.3. As a result, if the capacitance is tuned too much, maintaining a flat gain response becomes difficult for the designer. Therefore the usage of Technique 3 is only advisable when a relatively smaller gain tradeoff is desired. When a relatively larger SFDR improvement is desired and a larger gain sacrifice is afforded, Technique 1 can be combined with either Technique 2 or Technique 3. For demonstration of this, we applied Techniques 2 and 3 individually on our design example for Technique 1 in order to further improve the SFDR, while trading off more gain. Once again, for fair performance comparison between the two combinations, the gain was traded off equally (from 34.5 dBΩ to 30.0 dBΩ) in both cases. As can be observed from Table 4.2, the combination of Techniques 1 and 3 performs significantly better than the combination of Techniques 1 and 2 in terms of SFDR improvement, which is expected as Technique 3 alone has better gain to SFDR tradeoff performance compared to that of Technique 2 alone as we observed earlier. Hence we conclude that usage of a combination of Techniques 1 and 3 is advisable when a relatively larger SFDR is desired. In our design example, this combination resulted in a nett SFDR improvement of 9 dB with a nett 13.34 dBΩ gain tradeoff. Notably although

TABLE 4.1
SFDR AND TRANSIMPEDANCE GAIN COMPARISON BETWEEN THE REFERENCE DESIGN AND DESIGNS ALTERED USING THE THREE TECHNIQUES.

Simulation frequency	10 GHz		20 GHz		30 GHz	
	SFDR	Gain	SFDR	Gain	SFDR	Gain
Reference Design	68.0 dB	45.3 dBΩ	68.0 dB	45.6 dBΩ	66.3 dB	43.3 dBΩ
Technique 1 Design Example	71.9 dB	34.9 dBΩ	72.9 dB	34.3 dBΩ	71.8 dB	34.5 dBΩ
Technique 2 Design Example	68.8 dB	34.3 dBΩ	69.2 dB	35.2 dBΩ	70.3 dB	34.5 dBΩ
Technique 3 Design Example	69.1 dB	38.8 dBΩ	71.1 dB	36.9 dBΩ	71.8 dB	34.5 dBΩ

Technique 2 has the worst SFDR performance, it does not have the drawbacks of the other techniques, as it is both tunable and retains a flat gain response for the amplifier.

TABLE 4.2
SFDR TRANSIMPEDANCE GAIN COMPARISON BETWEEN DIFFERENT COMBINATIONS OF TECHNIQUES

Simulation frequency	10 GHz		20 GHz		30 GHz	
	SFDR	Gain	SFDR	Gain	SFDR	Gain
Technique 1 Design Example	71.9 dB	34.9 dBΩ	72.9 dB	34.3 dBΩ	71.8 dB	34.5 dBΩ
Techniques 1 and 2 combined	72.4 dB	30.3 dBΩ	73.2 dB	29.6 dBΩ	73.1 dB	30.0 dBΩ
Techniques 1 and 3 combined	73.9 dB	32.2 dBΩ	75.4 dB	30.7 dBΩ	75.3 dB	30.0 dBΩ

It will be noted that the combination of Techniques 2 and 3, or the combinations of all three techniques have not been attempted or demonstrated. This is because the combination of Techniques 2 and 3 in any single design would generally not be recommended due to reasons explained as follows. As the only drawback with Technique 1 is that it is not tunable, it is complimented by any of the other two techniques, when a large tradeoff is desired. However, Techniques 2 and 3 each have mutually exclusive performance related drawbacks. Technique 2 has a flat gain response, but relatively worse gain to SFDR tradeoff performance, while Technique 3 has good gain to SFDR tradeoff performance but sacrifices flat gain response to some extent. Depending on design preferences, the designer can choose between Technique 2 (flat gain response) or Technique 3 (better tradeoff value i.e. higher SFDR), and if a high tradeoff is desired, combine his choice of Techniques 2 or 3, with Technique 1. However, combining Techniques 2 and 3 in a single design, although possible to be implemented, would be ill advised because doing so would combine the drawbacks of the two techniques, and the design will have neither a flat gain response, nor the best

possible gain to SFDR tradeoff value. For the same reason, Techniques 1, 2 and 3 should also not be combined in a single design, although it is technically possible.

Notably, these techniques have not been experimentally validated. This was due to technical limitations of facilities available to the author. However, the author is confident of the validity of these methods as they have been theoretically reasoned, and then backed up through detailed, calibrated simulations, which fully agree with conclusions reached through theoretical reasoning. Moreover, the experimentally validated large signal model of a real transistor [45] was used rather than an ideal transistor for all simulations which adds further validity to our predictions and simulations. It should also be noted that the techniques have been compared using the same transistor model in all simulations in order to ensure that the comparisons were fair.

4.5 STABILITY CONSIDERATIONS

As is the general practice for amplifier design, the stability of the reference amplifier across frequency was considered during initial design using Rollett's stability factor method [108], and the amplifier was found to be unconditionally stable. The same method was also used to check any change in stability following each of the three techniques and the two combinations discussed in section 4.4. In all cases the amplifier was found to be unconditionally stable.

4.6 CONCLUSION

Three different novel methods of trading off transimpedance gain in order to improve the SFDR of HBT transimpedance distributed amplifiers were devised, discussed and demonstrated. Their performances were compared and the pros and cons of each method were presented. Performances of combinations of these methods were also compared and discussed. It was found that the Cascode Base Capacitor Adjustment Technique (Technique 3) offers the best tradeoff option in terms of SFDR performance when a relatively small gain tradeoff is desired, while a combination of the Emitter Follower Replacement Technique (Technique 1) and the Cascode Base Capacitor Adjustment Technique (Technique 3) is the best option when a relatively large SFDR improvement is desired. It was also found that the Amplifier Load Adjustment Technique (Technique 2) or a combination of Techniques 1 and 2 is the suitable tradeoff option when a flat gain response is desired.

As mentioned earlier, the three Techniques for SFDR improvement and their combinations introduced and demonstrated in this chapter are original contributions to the field of knowledge which were peer reviewed and accepted for publication in the PIER L journal in 2012 [107].

Chapter Five:

Transistor Design Options

5.1 INTRODUCTION

In Chapter 4 a number of techniques to improve the SFDR of HBT transimpedance distributed amplifiers in exchange of transimpedance gain on the circuit design level were established. However, given the fact that the transistors within the amplifier are the primary contributors to the non-linear behaviour of the amplifier, it is important to investigate the non-linear characteristics of the transistors themselves, especially how the nonlinearities are affected by transistor geometry and doping. Therefore in this chapter, keeping in mind that the gain and bandwidth of the amplifier are also a

priority along with the SFDR, we will focus on the influence of the geometry and doping of certain layers of the HBT transistor on the linearity, gain and f_T of the transistor.

It has been established that the good linear characteristics of HBTs are mainly caused by partial cancellation of intrinsic non-linear currents [54-56] and the feedback effect of the emitter and base resistances [57]. It is also well known that the non-linear nature of the base collector capacitance, C_{bc} is the dominant cause of nonlinearity in HBTs [56, 58–61]. As a solution to this problem, Kobayashi *et al.* in a previous work [62] suggested that in order to achieve maximum IP3 per unit DC power, $V_{depletion}$, which is the collector voltage at which full depletion occurs in the collector (therefore it is the collector voltage above which C_{bc} remains linear), can be lowered. It was briefly suggested in that work that this could be done by either reducing the thickness of the n-type collector region or by reducing the n-type doping in the collector. Over the following years, there have been a number of works in which the reduction of the collector thickness was successfully implemented to improve HBT linearity [63, 64], and this technique came to be known as the punch-through collector technique. However this solution is a tradeoff for OEIC applications, which we are focusing on, because reducing the collector thickness would also mean reducing the I-layer (intrinsic layer) in the PIN photodetector, which would result in reduced responsivity. In recent years there have also been a few works in which the employment of a high doping layer inside the collector in order to improve the HBT linearity was successfully introduced [65, 66]. However, this solution is also not suitable for OEIC applications, as it would compromise the uniformity of the I-layer of the PIN photodetector. On the other hand, there has also been work in which the reduction of

n-type doping in the collector was successfully used to improve HBT linearity [58]. This procedure has a positive side-effect on the PIN photodetector for OEIC applications, however it is important to investigate and understand the influence of this procedure on the gain and f_T of the transistor, which are the other two important figures of merit of the transistor which determines its suitability to be used in electronic warfare applications.

It has been shown in past work [67] that the doping of the spacer layer significantly influences HBT gain. Therefore it is also important to investigate the influence of the spacer layer attributes on the linearity, gain and f_T of HBTs because if it is found that the HBT gain can be improved by spacer layer manipulation without significant degradation of the f_T and linearity, it can be used to our advantage, as we have already developed tradeoff options between the gain and linearity of transimpedance HBT amplifiers as discussed in Chapter 4.

The influence of emitter width and base thickness of a HBT on its DC current gain and bandwidth has also been investigated recently [68]. It has been reported in that work that a higher emitter width, W_e results in higher f_T and thus higher bandwidth, while a higher Base thickness, X_B results in lower f_T and lower DC current gain. The results of this investigation also have the potential to be useful for the applications that we are focusing on. However, the influence of W_e and X_B on the linearity, AC current gain and AC forward voltage gain of the HBT, which are the other two figures of merit that are relevant to electronic warfare applications, has notably not been investigated. Therefore the influence of W_e and X_B on these figures of merit, namely the linearity and AC gain of a HBT is important to be investigated as well.

In this chapter, these various investigations were performed using the Silvaco TCAD [69] software. In Sections 5.2, 5.3 and 5.4 respectively, the reference design and the TCAD device simulation procedures that were used for the investigation are discussed, and the device simulation results are compared with measured results in order to demonstrate that the TCAD simulation results are accurate and reliable. In Section 5.5, the investigation of the influence of collector doping reduction on the gain and the f_T, along with the C_{bc} linearity of the HBT is carried out, and the results are presented and discussed. In Section 5.6, the influence of spacer layer doping and thickness on the gain, f_T and C_{bc} linearity is investigated and the results are discussed. In Section 5.7, the influence of the emitter width, W_e and base thickness, X_B on the gain, f_T and C_{bc} linearity is investigated and the results are discussed.

5.2 REFERENCE DEVICE DESIGN

As a starting point for each of our simulated investigations, we chose to use an InP/InGaAs HBT designed, fabricated and specified in detail by Tauqeer et al. [67] in 2008. The thicknesses and doping profiles of the epitaxial layers of the transistor as specified in [67] are shown in Table 5.1.

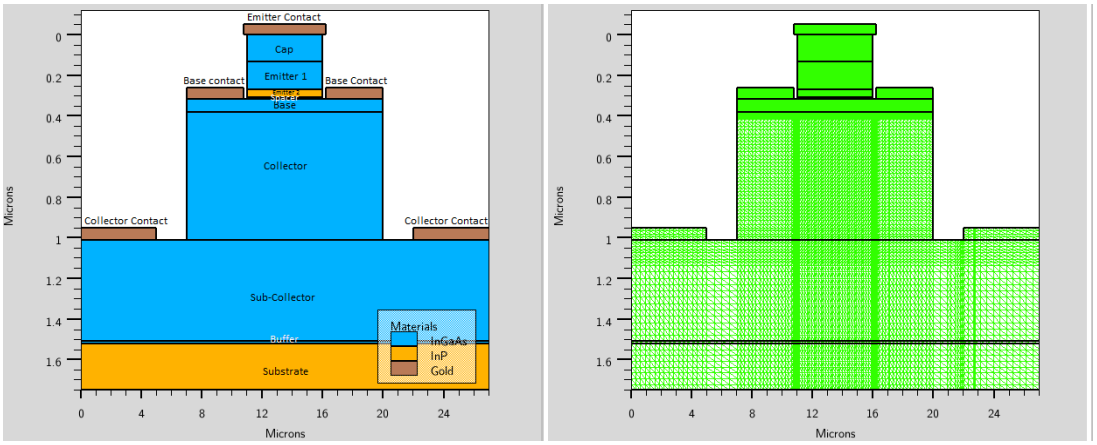
We used this transistor design as the reference transistor design for our device simulations in this work.

TABLE 5.1
SHBT EPILAYER STRUCTURE

Layer	MATERIAL	Doping(cm^{-3})	Thickness(A^o)
Cap	InGaAs	$n=1x10^{19}$	1350
Emitter 1	InGaAs	$n=1x10^{17}$	1350
Emitter 2	InP	$n=1x10^{17}$	400
Spacer	InGaAs	-	50
Base	InGaAs	$p=1.5x10^{19}$	650
Collector	InGaAs	$n=1x10^{16}$	6300
Sub-Collector	InGaAs	$n=1x10^{16}$	5000
Buffer	InGaAs	-	100
Substrate		Semi-Insulating InP	

5.3 DEVICE SIMULATION METHODOLOGY

The simulation software used in this study is the commercially available Silvaco TCAD software package [69], which is capable of high frequency simulation of III-V semiconductor devices. In order to simulate the transistor, the geometry, material and doping specifications of the transistor, stated in [67] were used to prepare the device for simulation. The device was carefully structured and meshed in the DEVEDIT module of the Silvaco software in order to maximize simulation accuracy and minimize software convergence errors during simulation, as shown in Figure 5.1.



(a) (b)

Figure 5.1: Structure of the Reference SHBT showing (a) All layers and (b) Meshing

The Silvaco TCAD software uses the ATLAS simulator module for modelling devices having materials from III-V or II-VI groups. Upon attempting to simulate the InP/InGaAs HBT transistor we noted that the current database of ATLAS is basically designed for the Silicon industry and as such does not incorporate the model parameters for III-V materials used in the device simulation models (listed below in sections 5.3.1-5.3.4) used for the simulations in this chapter. As a result, for the simulations to work for III-V materials, these model parameters, i.e. relevant material properties for the materials to be simulated are required to be manually entered in the source code of the simulation. From [67], we were able to acquire the values of most of the required material and model parameters for both InP and InGaAs, such as dielectric permittivity, bandgap, electron affinity, electron and hole saturation velocities, maximum and minimum mobility values at low and high doping levels for electrons and holes, etc. However, the values of some of the required model parameters were not available from [67] and were acquired for both InP and InGaAs through an extensive research of the literature, such as the critical electric field [98, 99], electron and hole lifetimes [100], Electron and hole Auger coefficients [101], etc.

The aforementioned device simulation models are listed and briefly discussed as follows. Each of them were included and used in all device simulations in this chapter.

5.3.1. Mobility models:

5.3.1.1. Caughey and Thomas mobility model:

This concentration dependent analytic mobility model is based on the Caughey and Thomas formula on effective mobility of electrons and holes [70].

5.3.1.2. Parallel Electric Field-Dependent Mobility model:

This model is used in order to take into account the effect of electric field on the mobility of the electrons and holes.

5.3.2. Recombination models:

5.3.2.1. Concentration dependant Shockley-Read-Hall model:

This model is included in order to account for carrier recombinations due to photon transitions, which occur in the presence of defects within the forbidden gap of the semiconductor. The model is based on the relevant theory that was first derived by Shockley and Read [71] and later by Hall [72]. The effect of impurity concentration on the carrier lifetimes is also taken into account.

5.3.2.2. Auger recombination model:

This model is included to take Auger recombinations into account in which the recombination of a single electron-hole pair causes a mobile carrier to be captured or emitted. This is an empirical model based on the following expression [73]:

Auger recombination,

$$R_{Auger} = AUGN\ (pn^2 - nn_{ie}^2) + AUGP\ (np^2 - pn_{ie}^2) \quad (5.1)$$

where *AUGN* and *AUGP* are electron and hole Auger coefficients respectively.

5.3.3. Carrier Statistics models:

5.3.3.1. Bandgap Narrowing model:

The presence of heavy doping in the base in HBTs causes a bandgap narrowing (BGN) effect, which results in a reduction of bandgap separation where the conduction band is lowered by roughly the same amount as the valence band is raised. This changes the intrinsic carrier density and disturbs the band offset, which leads to a change of the device characteristics [97]. As the base and cap layers of the reference HBT in this work are heavily doped (as observed in Table 5.1), bandgap narrowing will expectedly occur the effects of which needs to be taken into account, and for this purpose, the Bandgap Narrowing model is included.

5.3.3.2. Fermi-Dirac statistics model:

This model is used to predict the probability of an electronic state being occupied by an electron. It is based on the following expression [96]:

$$f(E) = 1/(1+exp((E-E_f)/kT)) \quad (5.2)$$

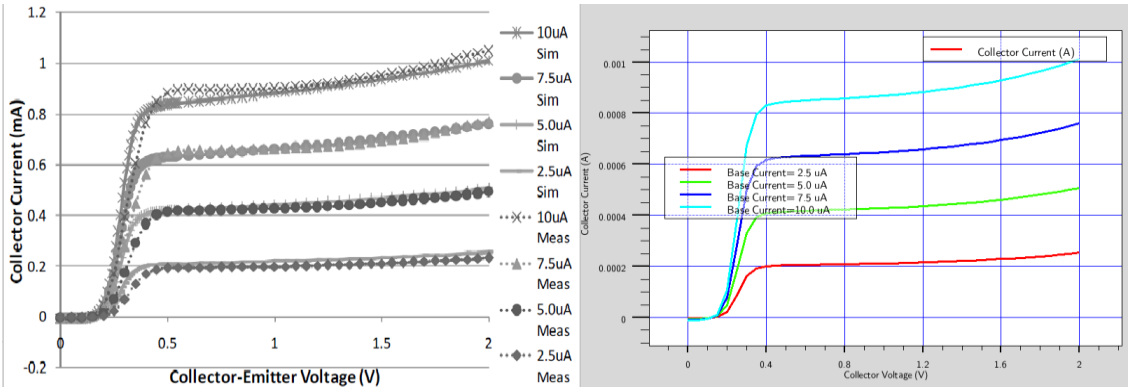
where $f(E)$ is the probability that an electron will occupy an electronic state with energy E, E_f is the Fermi level, k is the Boltzmann's constant and T is the absolute temperature.

5.3.4. Impact ionization model:

In order to simulate the impact ionization effect, the Selberherr's Model [74], which is based on the Chynoweth model [75], is implemented.

5.4 VALIDATION AGAINST MEASURED RESULTS

Due to the complex nature of TCAD device simulations, application of empirical models, and the fact that the simulations rely on numerous manually entered physical properties of semiconductors, which were obtained from a number of other works, these simulations are prone to producing inaccurate results resulting from convergence errors, technical limitations, misinterpretation of information gathered from other works, etc. Therefore it is important ensure that the relevant material properties and physical models to be used are correctly set up in the simulation. For this purpose, we simulated the reference SHBT transistor (5x5μm^2 emitter area) for its



(a) (b)

Figure 5.2: (a) Simulated and Measured I-V characteristics curves of the reference SHBT from [67]. (b) I-V characteristics curves of the reference SHBT acquired through Device Simulation in this work.

common emitter I-V characteristics and compared the results with measured I-V characteristics of the actual fabricated SHBT transistor of identical specification, which were presented in [67]. Simulated and measured common-emitter I-V characteristics of the reference SHBT are shown in Figure 5.2. As can be observed, the simulated results are identical to the measured results and this shows that the simulation parameters are set up correctly and the simulation results are reliable.

Notably, high frequency parameters such as S parameters of the device were not validated against measured results. This could not be done because measured high frequency parameters were not provided in [67] and were unavailable to the author as a result. However, the author is confident of the accuracy of the high frequency simulation results in this chapter due to reasons explained in section 5.9.

5.5 INFLUENCE OF COLLECTOR DOPING REDUCTION

As discussed in the introduction, the influence of the reduction of collector doping in order to improve linearity on the gain and f_T of the transistor is investigated in this section. For this investigation, four different n-type collector doping concentrations, namely 1.2e16 cm^{-3}, 1.0e16 cm^{-3}, 0.8e16 cm^{-3} and 0.6e16 cm^{-3} are used. Base collector capacitance, C_{bc} as a function of collector voltage, V_{ce} (at V_{be}=0V) for the different collector doping concentrations are shown in Figure 5.3(a). As can be observed from Figure 5.3(a) and Table 5.2, lower collector doping concentrations result in a lower $V_{depletion}$ value (which is derived from the C_{bc} vs V_{ce} plots as taught in

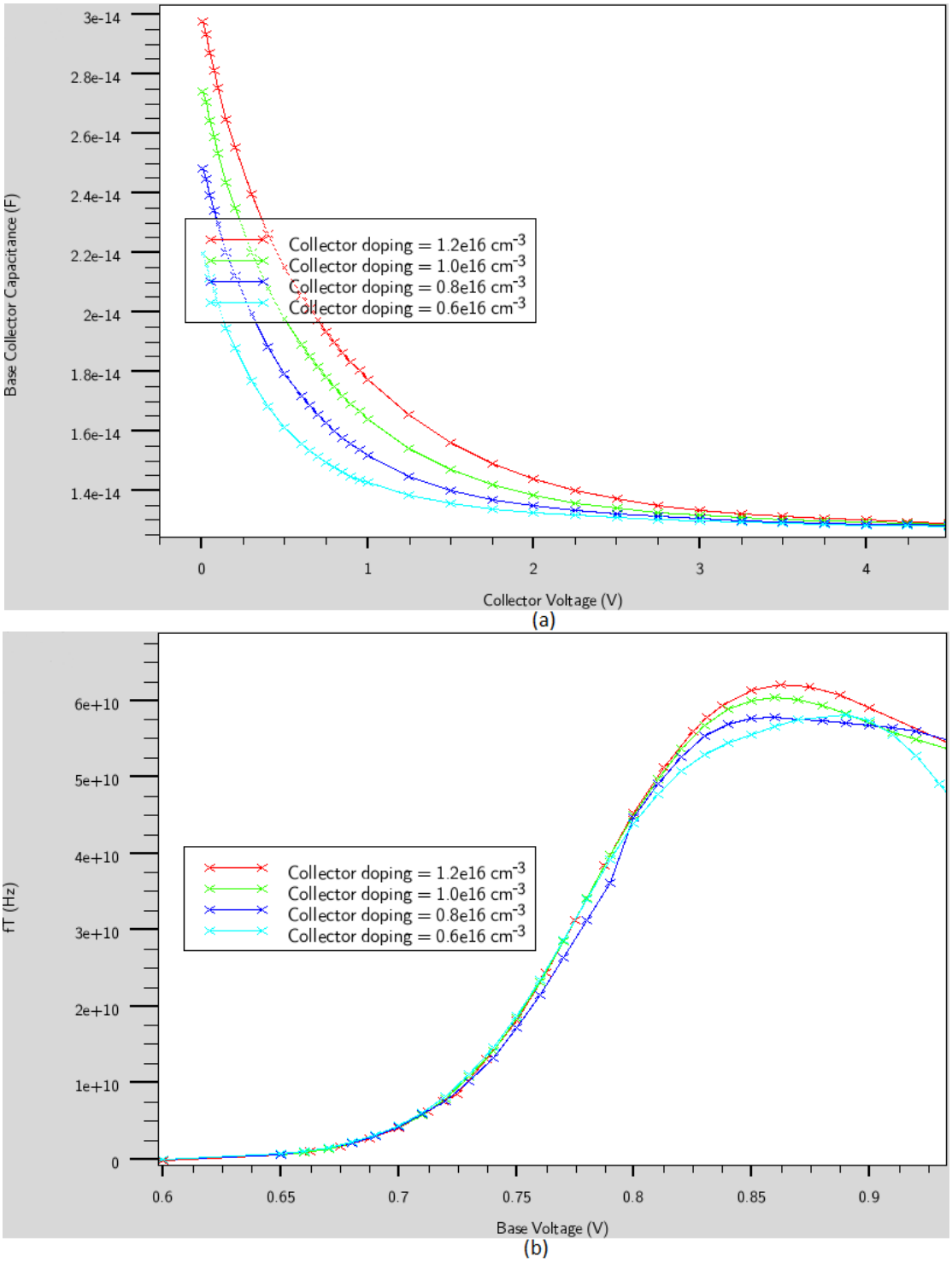


Figure 5.3: Results for four different collector doping profiles. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V).

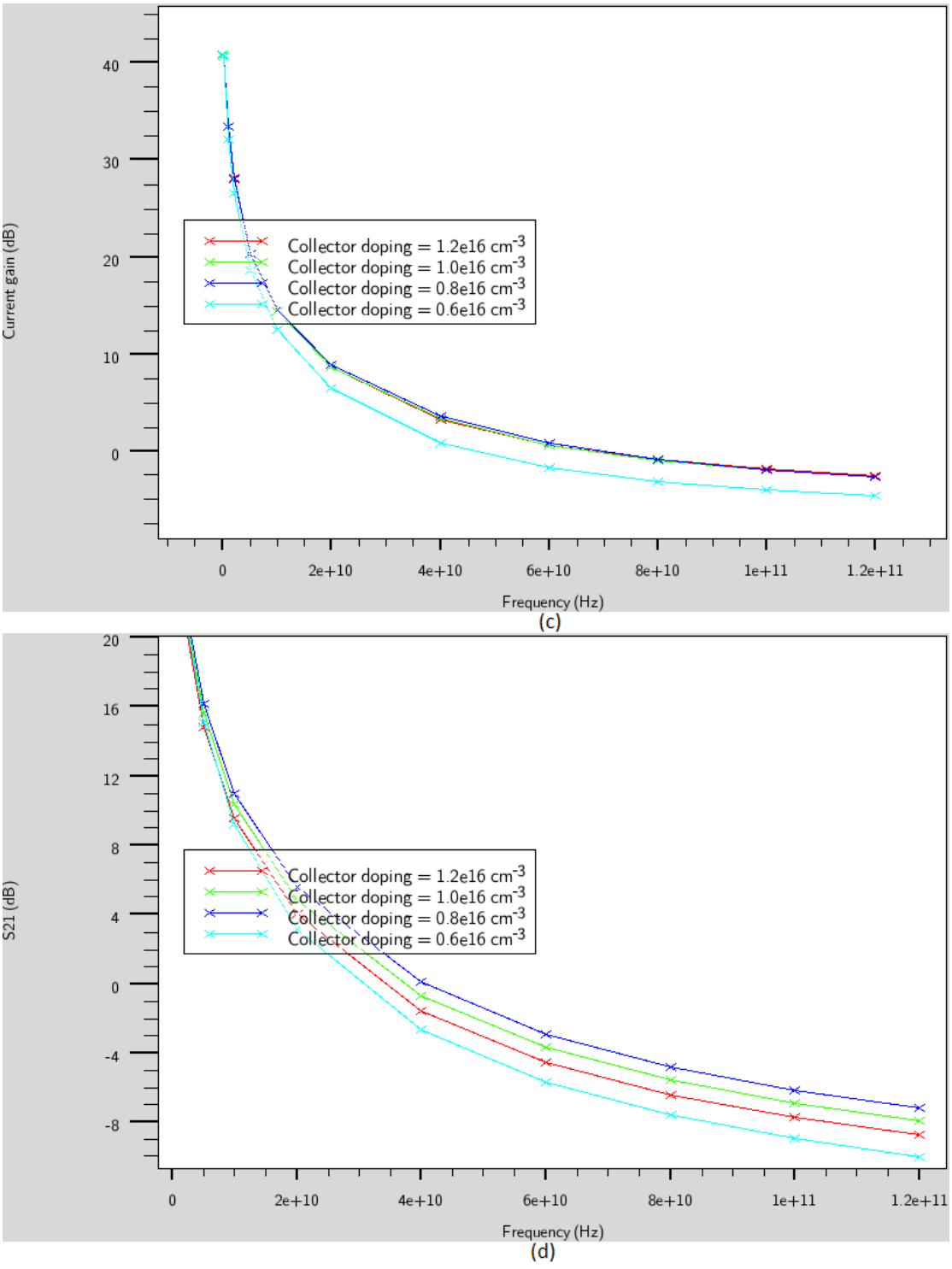


Figure 5.3 (continued): Results for four different collector doping profiles (at V_{be}=0.95V and V_{ce}=0.95V). (c) Current gain in dB versus frequency. (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V).

section III of [62]), which basically means better linearity of the HBT [56, 58–62]. However, the tradeoffs for this improvement of linearity are observed in Figures 5.3(b), 5.3(c) and 5.3(d). Figure 5.3(b) shows the unity current gain frequency, f_T of the transistor as a function of base voltage for the different collector doping concentrations. It is observed in this graph and Table 5.2 that lower collector doping concentrations result in a lower peak f_T value, which means the maximum frequency that can be achieved with the transistor is reduced. Notably, for all five investigations in this chapter (discussed in sections 5.5, 5.6, 5.7 and 5.8), the f_T was calculated through the following equation [103]:

$$f_t \approx \frac{g_m}{2\pi\left(C_{be} + C_{bc}\right)} \tag{5.3}$$

where, g_m, C_{be} and C_{bc} are the transconductance, base emitter capacitance and base collector capacitance respectively. These three parameters for different base voltage levels are determined through TCAD simulations.

Figures 5.3(c) and 5.3(d) show the current gain and the forward gain, $|S_{21}|$ (dB) of the transistor verses frequency respectively, with the transistor DC biased at V_{be}=0.95V and V_{ce}=0.95V. From these two graphs, it is observed that although the current gain remains relatively unchanged, the forward voltage gain rises with decreasing collector doping. However, the gain results for the doping concentration of 0.6e16 cm^{-3} appears to be an exception where both the current gain and forward voltage gain have significantly dropped. This suggests that there is a minimum collector doping concentration for a peak forward voltage gain. A possible reason which this drop in gain could be attributed to is the "base push out" or Kirk effect which occurs when the collector doping is too low, and which causes a drop in gain [102]. The author's

estimation in this case is that the gain rises with decreasing collector doping due to decreasing base collector capacitance until a certain limit beyond which the Kirk effect starts to take effect and the gain starts to fall.

5.6 INFLUENCE OF SPACER DOPING AND THICKNESS VARIATION

5.6.1 Spacer Doping Variation

As already mentioned in the introduction, Tauqeer et al. in 2008 [67] showed that increasing the doping of the spacer layer of HBTs results in higher transistor gain. This is of interest to us because we have established in Chapter 4 that the gain of HBT transimpedance distributed amplifiers (which we determined to be the ideal amplifier topology for use in OEIC receivers in electronic warfare applications in Chapter 3) can be traded off for amplifier linearity and dynamic range. Therefore the effect of increasing the spacer doping to improve the transistor gain on the linearity and the f_T of the transistor is of importance and will be investigated in this section. Four different p-type spacer doping concentrations, namely 0 cm^{-3} (intrinsic), 5e18 cm^{-3}, 10e18 cm^{-3} and 14e18 cm^{-3} are used for this investigation. Base collector capacitance, C_{bc} as a function of collector voltage for the different doping concentrations are shown in Figure 5.4(a). As can be observed from Figure 5.4(a) and Table 5.3, changing spacer doping concentrations result in almost no change in the $V_{depletion}$ value, which basically means the linearity of the HBT is unaffected. Figure 5.4(b) shows the unity current gain frequency, f_T of the transistor (determined based on equation 5.3) as a function of base voltage for the different spacer doping concentrations. It is observed in this graph and Table 5.3 that higher spacer doping

concentrations result in a higher peak f_T value, which suggests that a higher amplifier bandwidth can be achieved with the transistor.

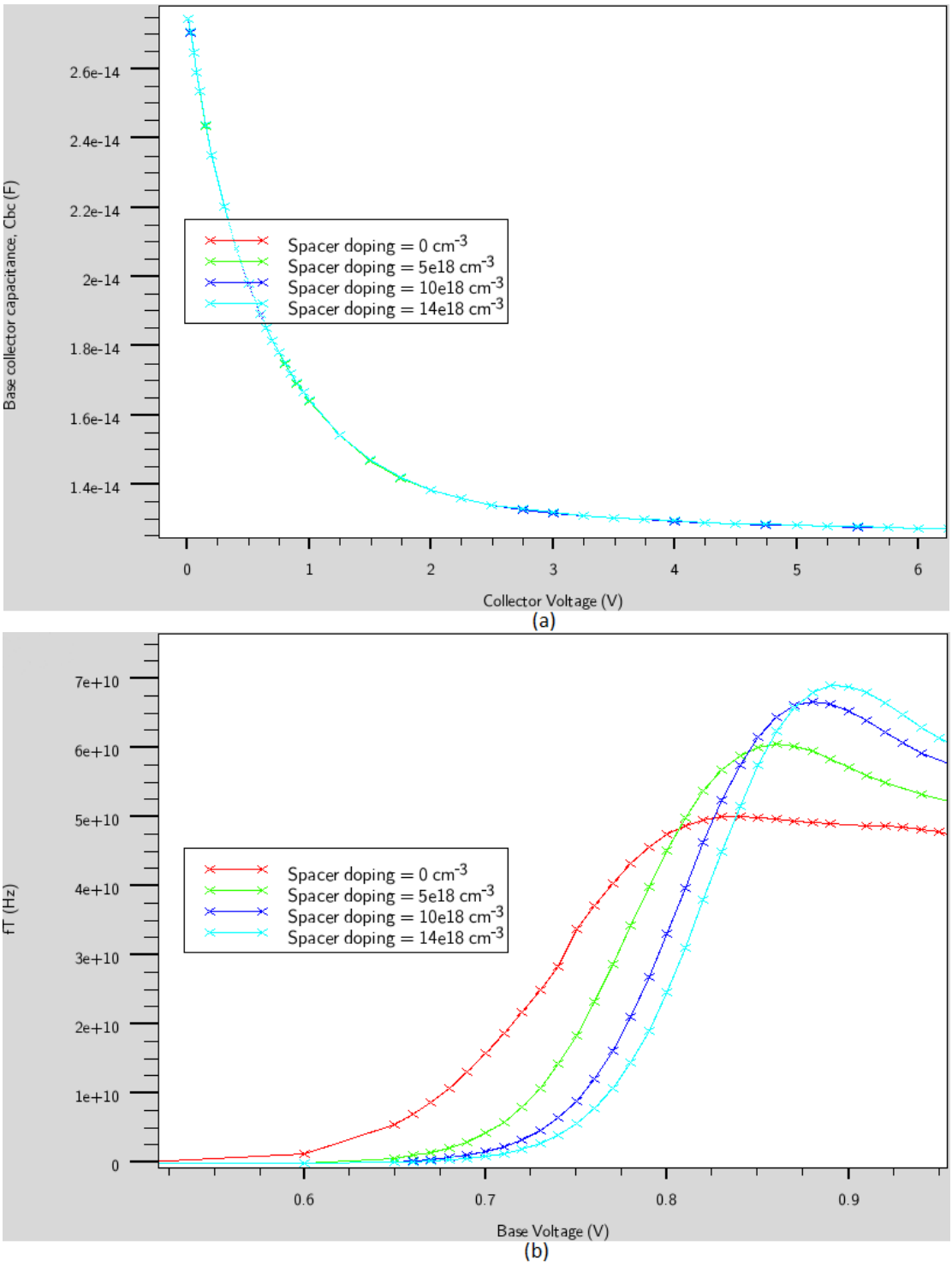
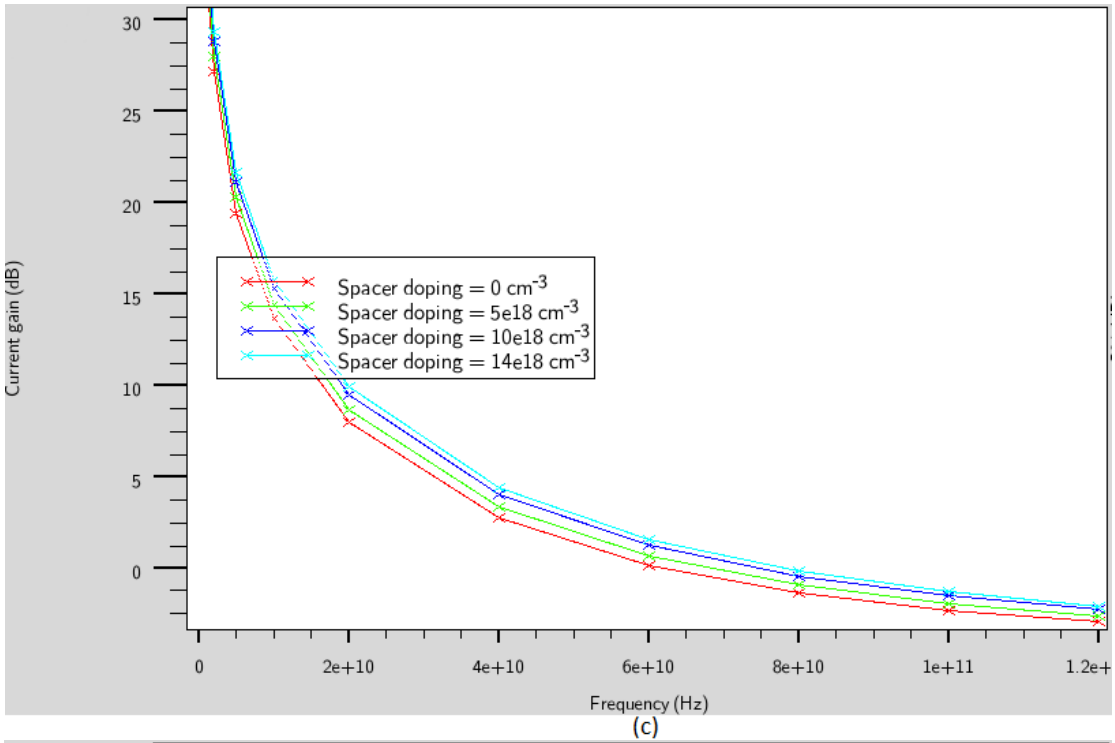
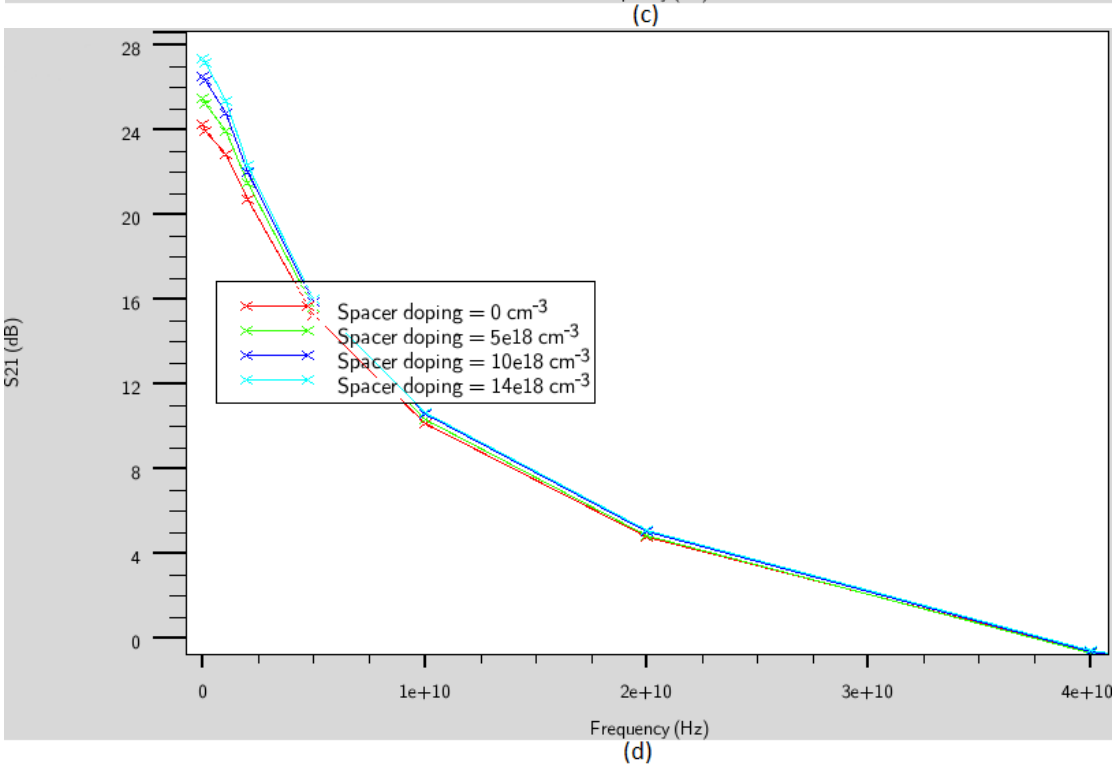


Figure 5.4: Results for four different spacer doping profiles. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V).



(c)



(d)

Figure 5.4 (continued): Results for four different spacer doping profiles. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V).

Figures 5.4(c) and 5.4(d) show the current gain and the forward voltage gain, $|S_{21}|$ (dB) of the transistor versus frequency respectively, with the transistor DC biased at V_{be}=0.95V and V_{ce}=0.95V. From these two graphs, it is observed that as predicted in [67], both the current gain and the forward voltage gain rises with increasing spacer doping due to reduced recombination in the narrow-bandgap spacer region. Therefore we conclude that increasing the spacer p-type doping results in increased gain and f_T with no negative effects on the linearity of the HBT. However it should be noted that increasing the spacer doping beyond a certain level will cause the layer to no longer function as a spacer layer, and therefore limits should apply beyond which the doping should not be increased.

5.6.2 Spacer Thickness Variation

The influence of spacer layer thickness on the linearity, f_T and gain of HBTs will now be investigated. For this investigation, the C_{bc} linearity, f_T, current gain and forward voltage gain of the reference HBT is tested for four different spacer layer thicknesses, namely 2 nm, 5 nm, 10 nm and 15 nm, the results of which are shown in Figure 5.5. As we can observe from Figure 5.5(a), varying the spacer layer thickness has negligible effect on C_{bc} linearity and $V_{depletion}$, which suggests it has no effect on the linearity of the HBT. Similarly, Figure 5.5(b) shows that the maximum f_T value (determined based on equation 5.3) remains relatively unchanged for the four cases. Figures 5.5(c) and 5.5(d) on the other hand show that the current gain and the forward voltage gain of the HBT are increased for higher spacer layer thickness values. However, the gain results for the spacer layer thickness of 15nm appears to be an exception where both the current gain and forward voltage gain have significantly dropped, presumably because the spacer layer is now so thick that it no longer

behaves as such. This suggests that there is a maximum spacer layer thickness for a peak transistor gain. These results are summarized in more detail in Table 5.4.

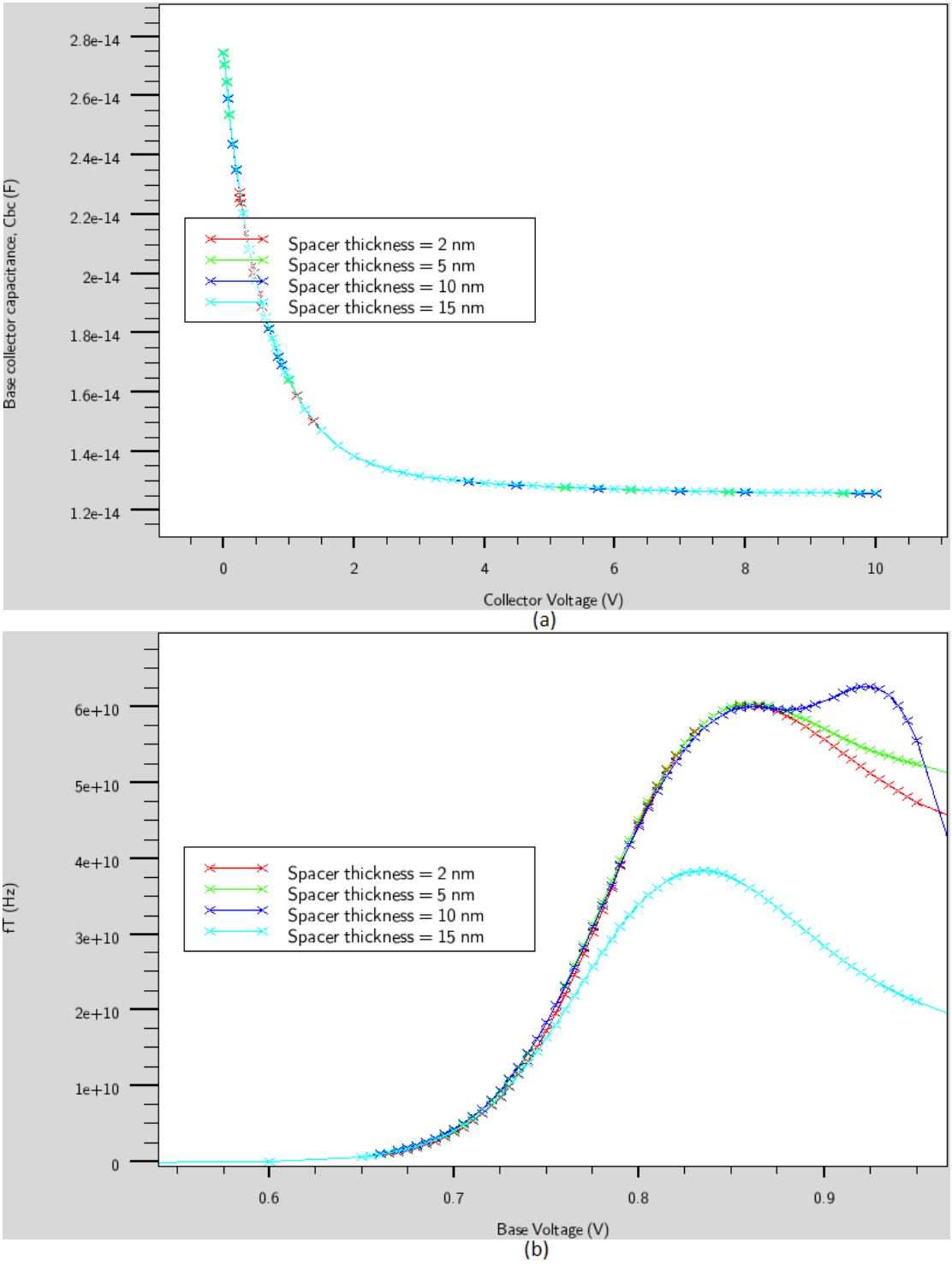
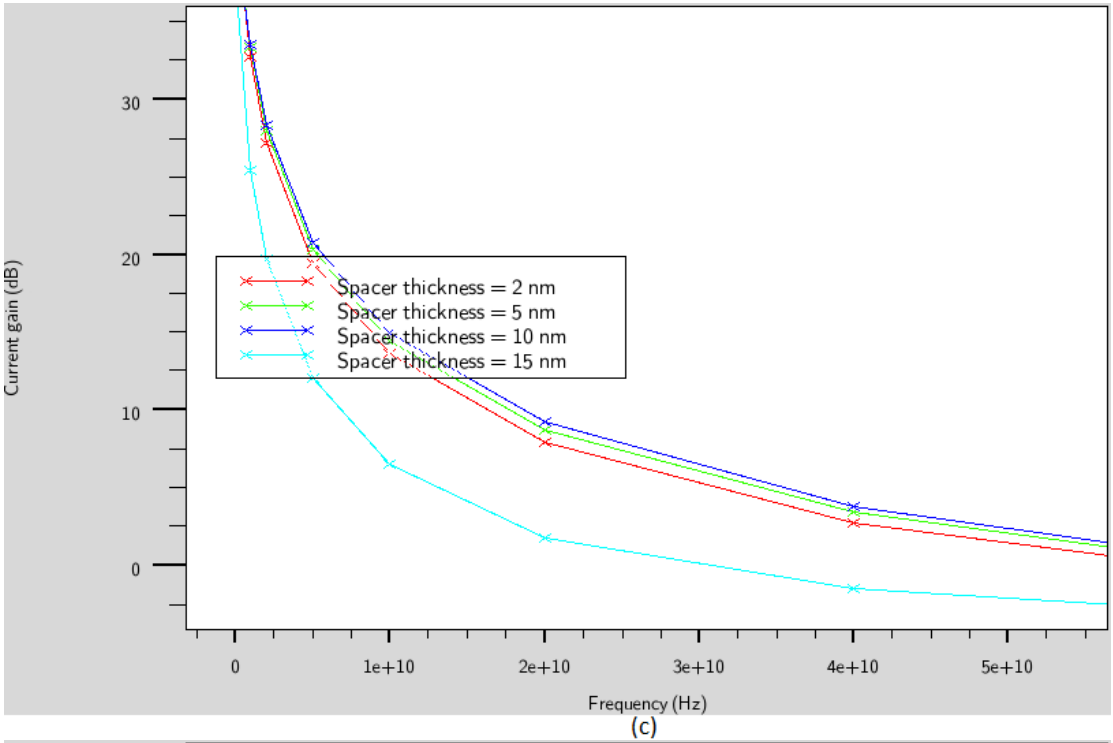
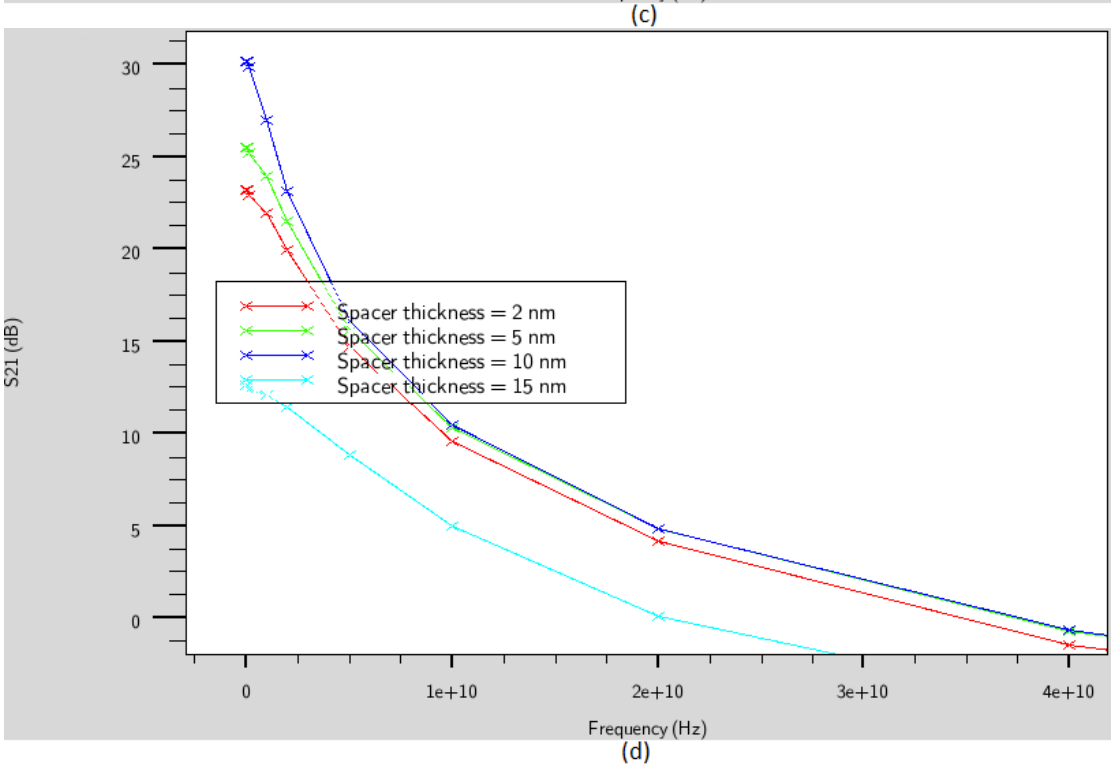


Figure 5.5: Results for four different spacer thicknesses. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V).



(c)



(d)

Figure 5.5 (continued): Results for four different spacer thicknesses. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V).

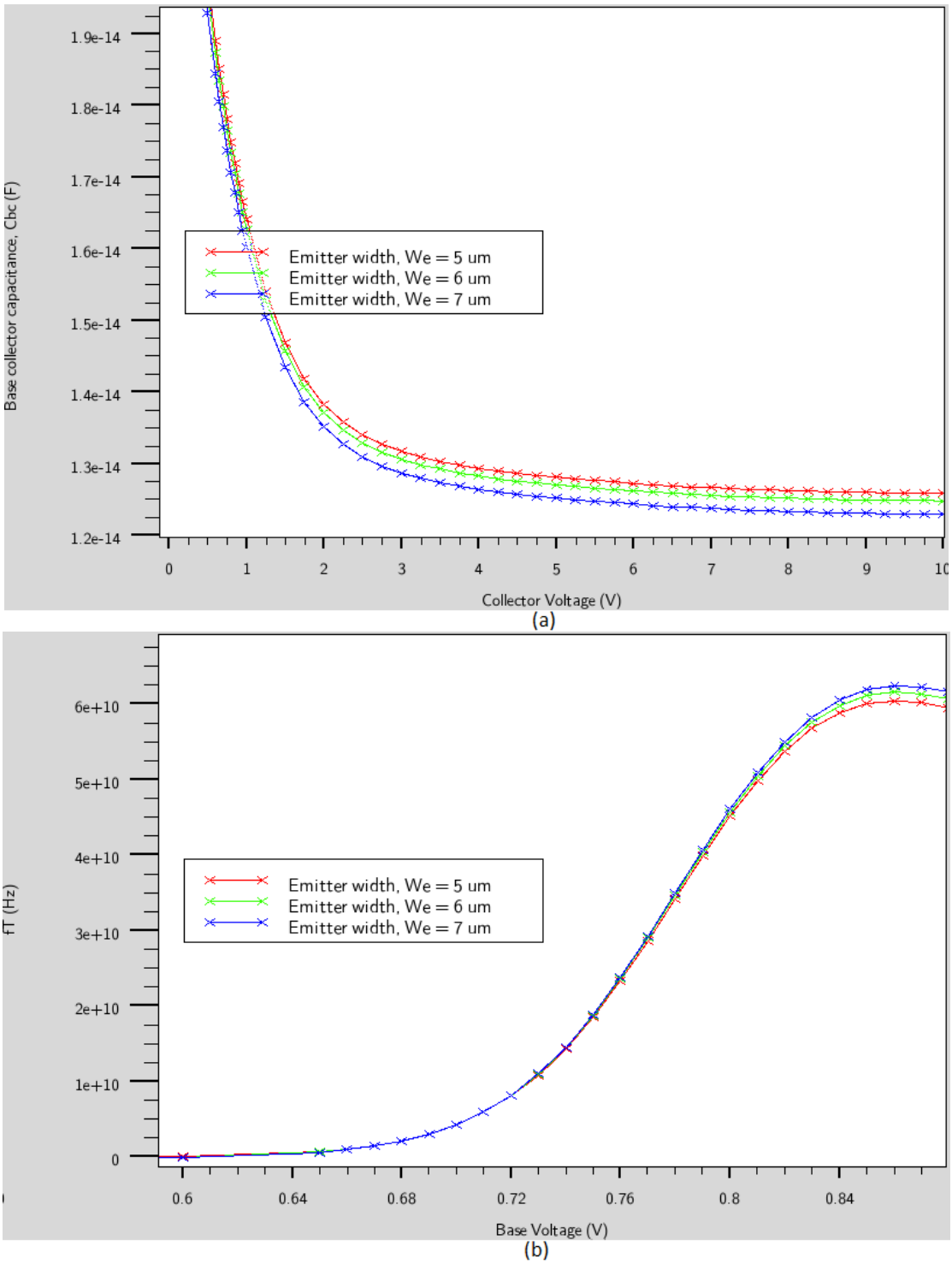
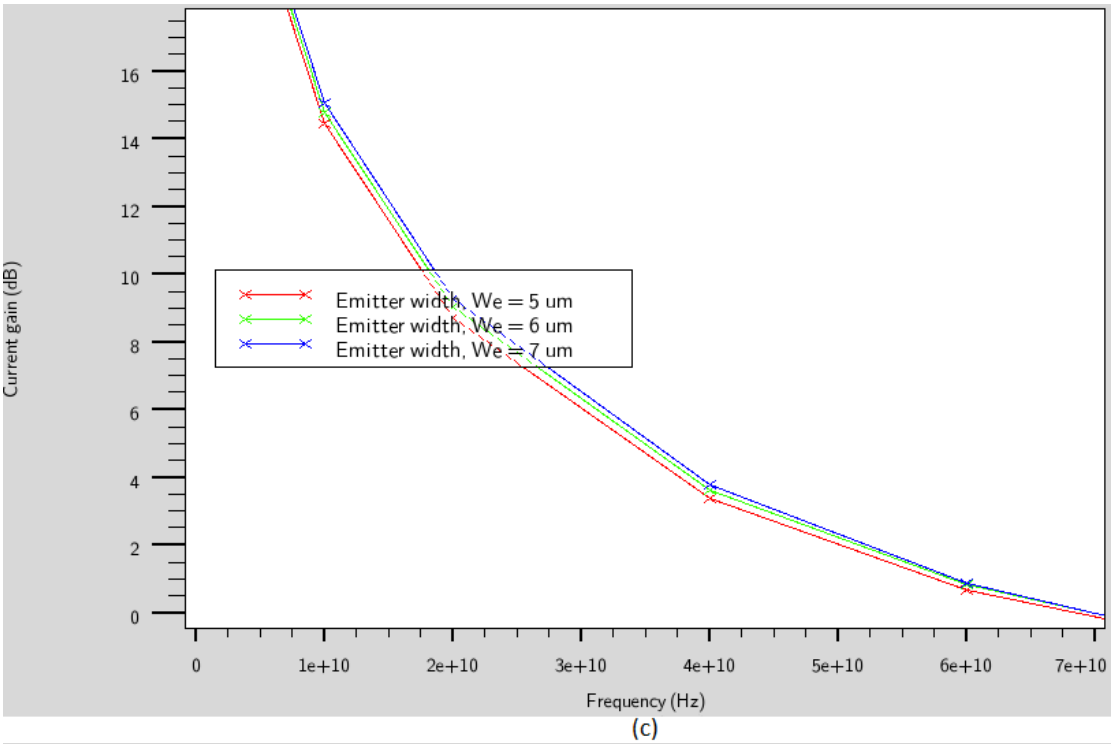
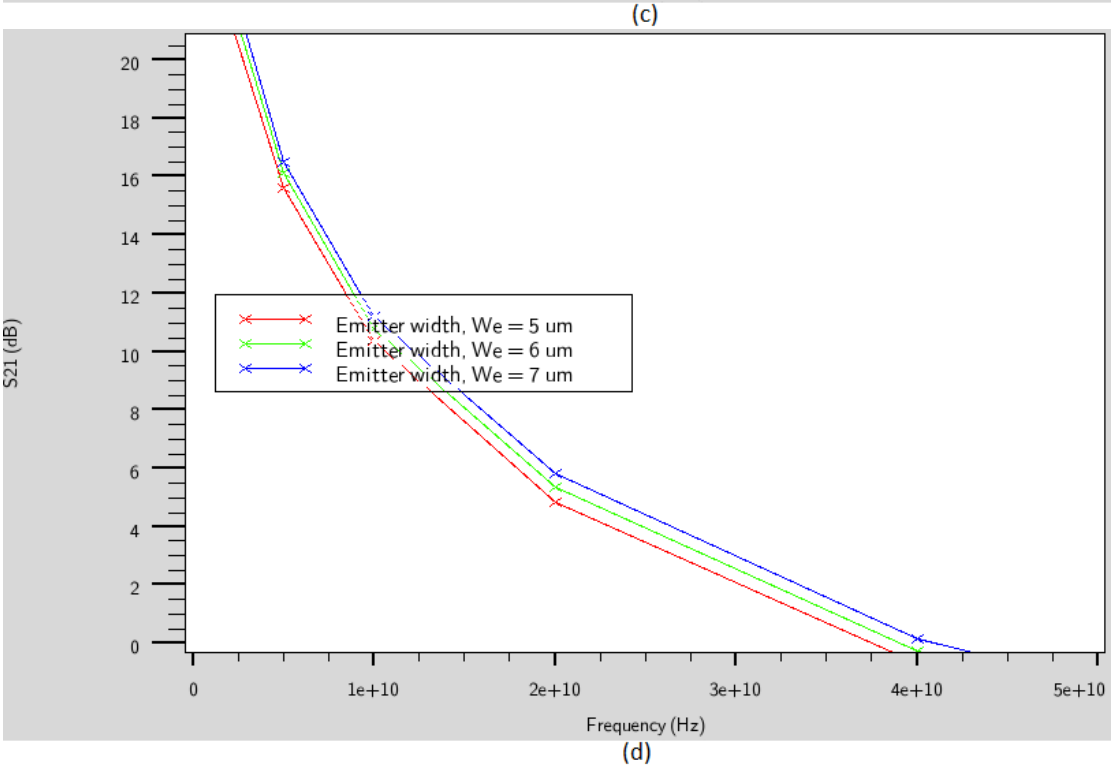


Figure 5.6: Results for three different emitter widths. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V).



(c)



(d)

Figure 5.6 (continued): Results for three different emitter widths. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V).

5.7 EMITTER WIDTH AND BASE THICKNESS VARIATION

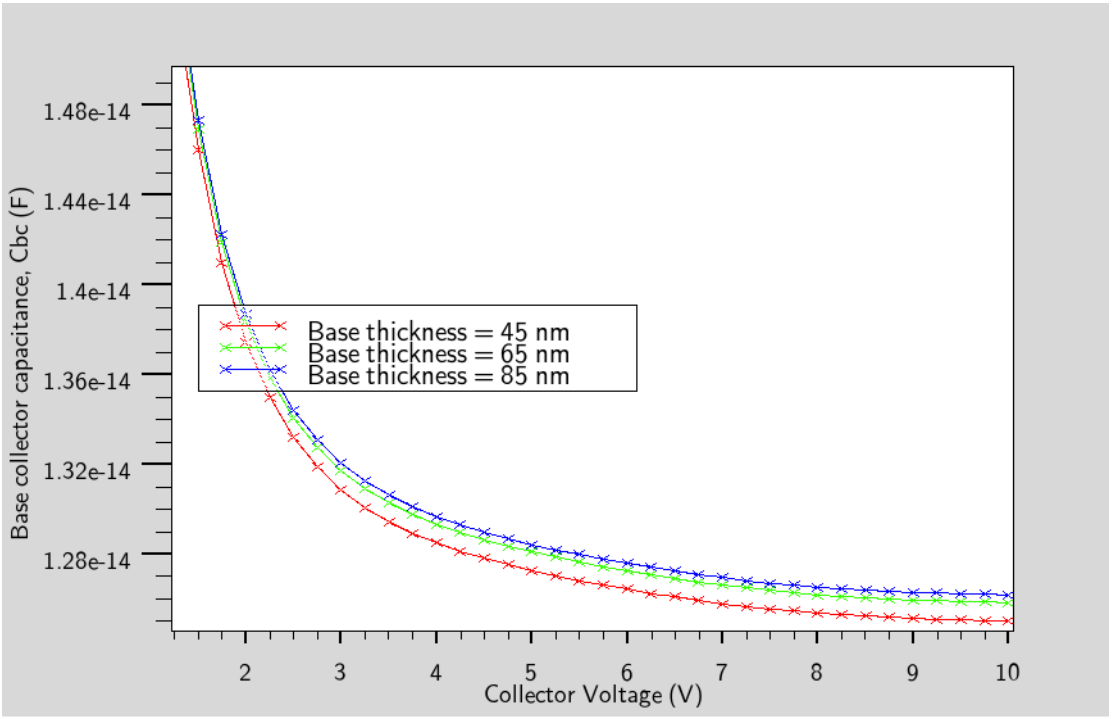
5.7.1 Emitter Width Variation

The influence of the width of the emitter, W_e on the linearity, f_T and gain of HBTs is investigated in this subsection. For this investigation, the C_{bc} linearity, f_T, Current gain and forward voltage gain of the reference HBT are tested for three different emitter width values, namely 5 μm, 6 μm and 7 μm, the results of which are shown in Figure 5.6. As we can observe from Figure 5.6(a), a higher emitter width results in a noticeably lower C_{bc} value and a lower $V_{depletion}$ value indicating an improvement in linearity. Figures 5.6(b), 5.6(c) and 5.6(d) respectively show that the f_T (determined based on equation 5.3), current gain and forward voltage gain of the HBT are also improved when the emitter of the HBT is made wider. These results are summarized in more detail in Table 5.5.

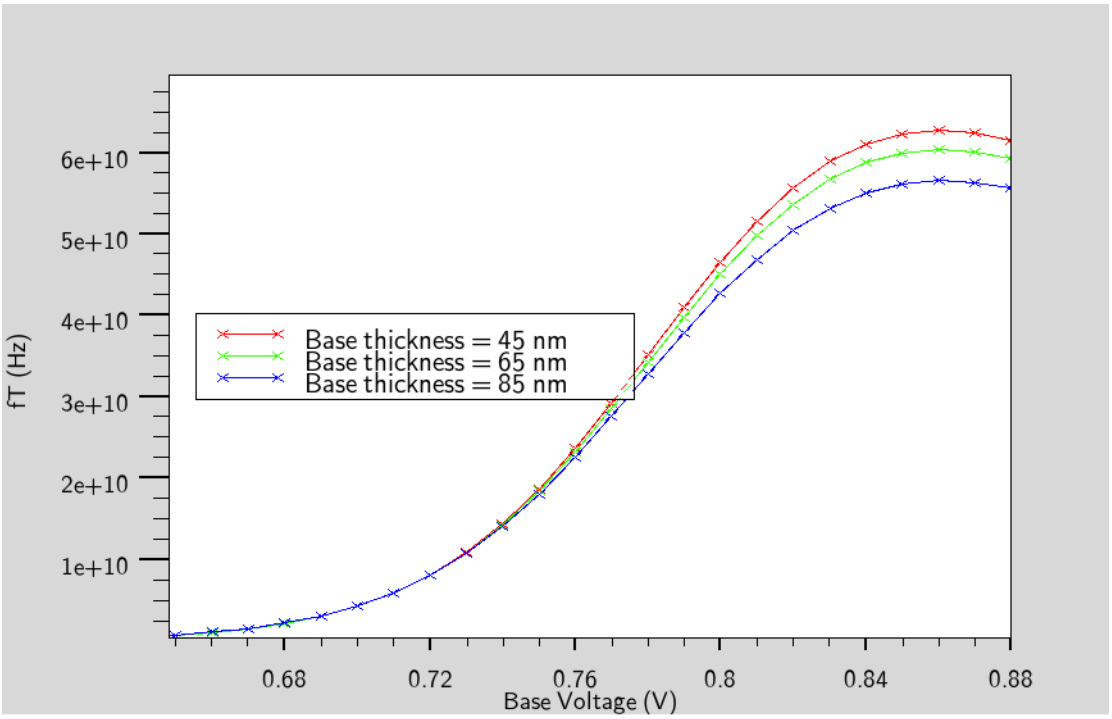
5.7.2 Base Thickness Variation

The influence of the thickness of the base, X_B on the linearity, f_T and gain of HBTs is investigated in this subsection. For this investigation, the C_{bc} linearity, f_T, Current gain and forward voltage gain of the reference HBT are tested for three different X_B values, namely 45 nm, 65 nm and 85 nm, the results of which are shown in Figure 5.7. As we can observe from Figure 5.7(a), decreasing the thickness of the base causes C_{bc} to drop and the $V_{depletion}$ value is also observed to drop significantly indicating an improvement in linearity. Figures 5.7(b), 5.7(c) and 5.7(d) show that this also causes

the HBT to have an improved bandwidth (determined based on equation 5.3), current gain and forward voltage gain performance. These results are detailed in Table 5.6.

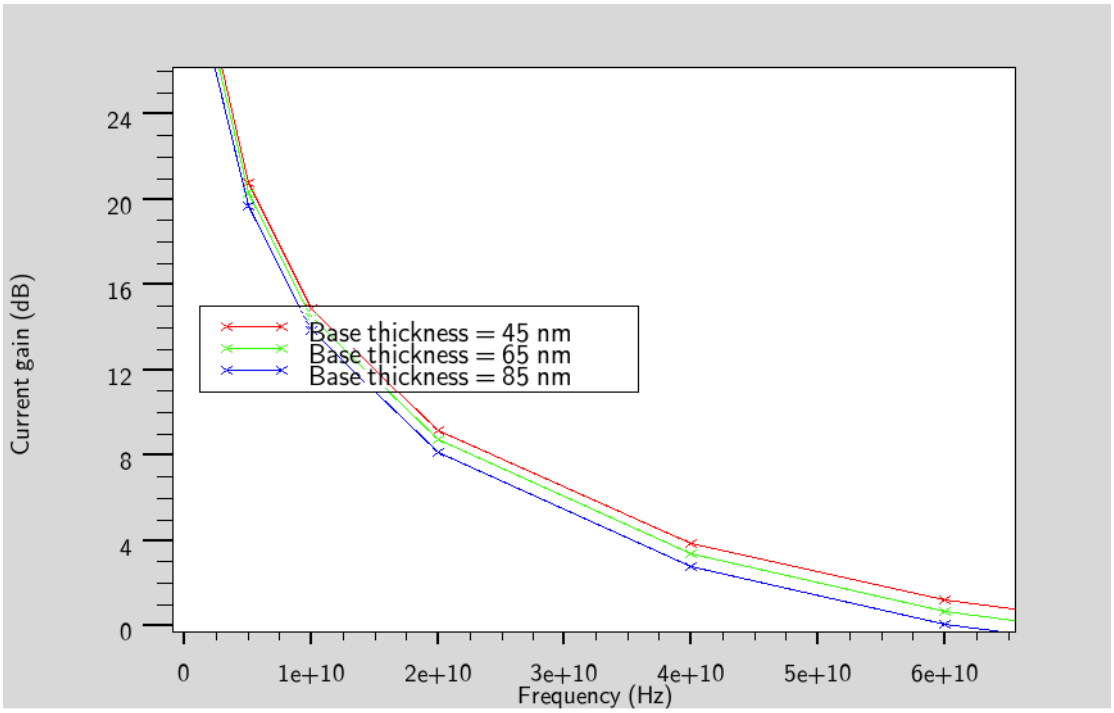


(a)

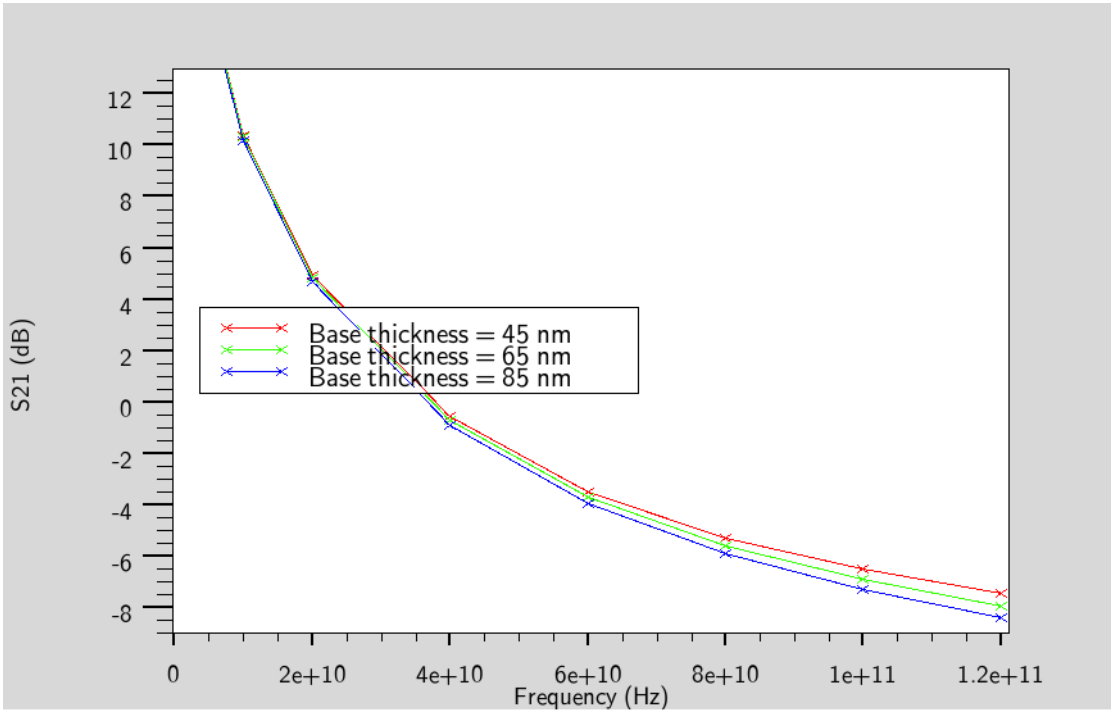


(b)

Figure 5.7: Results for three different base thicknesses. (a) Base Collector Capacitance C_{bc} versus Collector voltage (at V_{be}=0V). (b) Unity current gain frequency, f_T verses Base voltage (at V_{bc}=0V).



(c)



(d)

Figure 5.7 (continued): Results for three different base thicknesses. (c) Current gain in dB versus frequency (at V_{be}=0.95V and V_{ce}=0.95V). (d) Forward gain, S_{21} versus frequency (at V_{be}=0.95V and V_{ce}=0.95V).

5.8 RESULTS AND DISCUSSION

Tables 5.2, 5.3, 5.4, 5.5 and 5.6 summarize the results that were discussed in Sections 5.5, 5.6 and 5.7. Table 5.2 shows the effect of using reduced collector doping concentration on the linearity, bandwidth and gain of the HBT. As can be observed in Table 5.2, using reduced collector doping results in a significantly lower $V_{depletion}$ value, which according to [56, 58-61] and especially [62] essentially means that linearity is improved. This result was expected because it had already been predicted by Kobayashi in [62], and this work serves to confirm that prediction. However, the side effects of such reduction of collector doping in order to improve the linearity of a HBT on the f_T and gain of the transistor has not been investigated in the literature to the best of the authors' knowledge. As discussed in the introduction, these investigations are important especially for our application of interest, as the gain and bandwidth of the transistor are just as important as its linearity in electronic warfare applications. Table 5.2 shows that a reduction of collector doping results in lower f_T, which would result in a lower amplifier bandwidth. However, it is also observed that the reduction of collector doping results in a higher transistor gain, to a certain point below which the reduction of the collector doping results in the layer no longer behaving as the collector layer and as a result the gain drops sharply. Therefore we conclude that this procedure can be used to enhance the linearity and gain of the transistor, at the cost of bandwidth.

TABLE 5.2
SUMMARY OF THE INFLUENCE OF COLLECTOR DOPING CONCENTRATION ON THE LINEARITY, BANDWIDTH AND GAIN OF INP HBTS

Collector doping	$V_{depletion}$	Unity current gain frequency, f_T	Current gain at 10 GHz	Forward voltage gain, |S21| at 10 GHz
1.2e16 cm^{-3}	3.1 V	62.0 GHz	14.45 dB	9.56 dB
1.0e16 cm^{-3}	2.7 V	60.4 GHz	14.45 dB	10.34 dB
0.8e16 cm^{-3}	2.3 V	57.8 GHz	14.55 dB	10.95 dB
0.6e16 cm^{-3}	1.9 V	58.1 GHz	12.56 dB	9.24 dB

Table 5.3 shows the influence of spacer layer doping on the linearity, f_T and gain of the HBT. $V_{depletion}$ is unchanged with varying spacer layer doping, which basically means that the Spacer layer doping has negligible influence on the linearity of the transistor. However both the f_T and the gain of the transistor are higher at higher spacer layer doping. Therefore we learn that increasing spacer layer doping can be

TABLE 5.3
SUMMARY OF THE INFLUENCE OF SPACER DOPING CONCENTRATION ON THE LINEARITY, BANDWIDTH AND GAIN OF INP HBTS

Spacer doping	$V_{depletion}$	Unity current gain frequency, f_T	Current gain at 10 GHz	Forward voltage gain, |S21| at 10 GHz
0 (Intrinsic)	2.7 V	50.0 GHz	13.65 dB	10.11 dB
5e18 cm^{-3}	2.7 V	60.4 GHz	14.45 dB	10.34 dB
10e18 cm^{-3}	2.7 V	66.6 GHz	15.31 dB	10.57 dB
14e18 cm^{-3}	2.7 V	68.9 GHz	15.80 dB	10.68 dB

used to not only enhance gain, as previously shown by Tauqeer in [67], but also the bandwidth of HBTs, with no degradation of its linearity characteristics.

TABLE 5.4
SUMMARY OF THE INFLUENCE OF SPACER LAYER THICKNESS ON THE LINEARITY, BANDWIDTH AND GAIN OF INP HBTS

Spacer thickness	$V_{depletion}$	Unity current gain frequency, f_T	Current gain at 10 GHz	Forward voltage gain, |S21| at 10 GHz
2 nm	2.7 V	60.3 GHz	13.59 dB	9.60 dB
5 nm	2.7 V	60.4 GHz	14.45 dB	10.34 dB
10 nm	2.7 V	62.9 GHz	14.91 dB	10.44 dB
15 nm	2.8 V	38.4 GHz	6.49 dB	4.99 dB

Table 5.4 shows the effect of having a thicker spacer layer on the linearity, bandwidth and gain of the HBT. It is observed that to a certain limit, a thicker spacer layer results in a higher f_T and gain of the HBT, while having no negative effects on its linearity, as $V_{depletion}$ appears to be unchanged with increasing spacer layer thickness. Therefore this may also be used to advantage during the design of the HBT structure for relevant applications.

Table 5.5 shows the effect of having a wider emitter on the linearity, bandwidth and gain of the HBT. It is observed that a wider emitter section results in a higher f_T and therefore bandwidth of the HBT. This result is expected because it is as previously predicted by Kaatuzian's investigations [68], and shows that the bandwidth can be

improved by making the emitter section wider. However, the influence of this procedure on the AC gain and linearity in the HBT has not been investigated until now despite their importance in analogue OEIC applications. Table 5.5 shows that making the emitter section wider also improves the current gain and the forward voltage gain of the transistor. A lower $V_{depletion}$ value for wider emitter sections suggests that it improves the linearity of the HBT as well. Therefore we conclude from this work that wider emitter sections can be used to improve the linearity, bandwidth, current gain and voltage gain of HBT transistors to a certain limit as allowed by fabrication complexity and overall size of the HBT.

TABLE 5.5
SUMMARY OF THE INFLUENCE OF EMITTER WIDTH ON THE LINEARITY, BANDWIDTH AND GAIN OF INP HBTS

Emitter width	$V_{depletion}$	Unity current gain frequency, f_T	Current gain at 10 GHz	Forward voltage gain, |S21| at 10 GHz
5 μm	2.70 V	60.4 GHz	14.45 dB	10.34 dB
6 μm	2.51 V	61.5 GHz	14.79 dB	10.80 dB
7 μm	2.19 V	62.4 GHz	15.06 dB	11.21 dB

Table 5.6 shows how the base thickness, X_B, influences the linearity, bandwidth and gain performance of the HBT. From [68, 112], we know that increasing X_B in a HBT results in lower DC current gain. This is confirmed by our simulations as we found that the DC current gain for X_B values of 45 nm, 65 nm and 85 nm resulted in DC current gain values of 48.50 dB, 40.72 dB and 35.81 dB respectively. Investigations in this work further revealed that the AC current and voltage gains are affected similarly by this increase, as is observed in Table 5.6. We also note that the $V_{depletion}$ value is

reduced significantly with decreasing X_B, indicating that the linearity improves with lower base thickness, and that the f_T value is improved by 6.1 GHz for a 40 nm reduction of X_B, which indicates a significant bandwidth improvement. Therefore we conclude from this table that X_B reduction can be used to improve all four FOMs, i.e. the linearity, bandwidth, AC current and voltage gain performance of a HBT. However, the disadvantage of X_B reduction is that it results in higher base sheet resistance [7, 112] which leads to parasitic effects which in turn causes the high frequency performance of the transistor to suffer, as a low base sheet resistance is required for high frequency transistor operation [113]. Thus the adjustment of X_B is a tradeoff between the abovementioned improvements and low parasitics.

TABLE 5.6
SUMMARY OF THE INFLUENCE OF BASE THICKNESS ON THE LINEARITY, BANDWIDTH AND GAIN OF INP HBTS

Base thickness	$V_{depletion}$	Unity current gain frequency, f_T	Current gain at 10 GHz	Forward voltage gain, |S21| at 10 GHz
45 nm	2.05 V	62.7 GHz	14.89 dB	10.38 dB
65 nm	2.70 V	60.4 GHz	14.45 dB	10.34 dB
85 nm	4.32 V	56.6 GHz	13.88 dB	10.17 dB

5.9 VALIDITY OF FINDINGS IN ABSENSE OF MEASURED RESULTS

While the validity of the simulation results may be questioned in the absence of measured results, the author believes these simulations to be substantially accurate based on the following:

1. The I-V characteristics of the simulated HBT were compared with measured I-V characteristics of a HBT of identical specifications, and an almost perfect match was observed, as presented in Figure 5.2.

2. The gain of the simulated HBT was found to respectively rise and drop with increasing and decreasing p-type spacer doping as can be observed in Figure 5.4, which conforms with conclusions reached through measured results in [67].

3. The f_T of the simulated HBT was found to rise with increasing emitter width, as can be observed in Table 5.5, which conforms with conclusions reached through the physically based theoretical analysis in [68].

4. The influence of modification of base thickness on both the f_T and DC current gain of the simulated HBT as observed in Table 5.6 was found to conform precisely with the conclusions reached through the physically based theoretical analysis in [68] and experimentally measured results in [112].

5. Reducing the n-type collector doping resulted in a lower $V_{depletion}$ value as predicted by Kobayashi et al. through theoretical analysis [62].

Therefore conformance with measured experimental results and results derived from theoretical analysis published in the prior art is observed in five different instances while at the same time no discrepancies or contradictions with the prior art were encountered, which in the balance of probabilities form reasonably significant evidence that the simulations are valid and realizable.

5.10 RECOMMENDATIONS BASED ON RESULTS

Based on the findings summarized in section 5.8, a series of recommendations is made for the reference transistor in light of the overall objectives of this project summarized in section 1.3 (i.e. improved linearity, gain and bandwidth of the amplifier) in Table 5.7. The aim of these recommendations is to present directions to modify the reference transistor in ways that would best accomplish the goals of the project.

TABLE 5.7
SUMMARY OF RECOMMENDED MODIFICATIONS TO DEVICE SPECIFICATIONS

	Original device	Proposed device
Collector doping	1e16 cm^{-3}	0.8e16 cm^{-3}
Spacer doping	Intrinsic	10e18 cm^{-3}
Spacer layer thickness	5 nm	10 nm
Emitter width	5 um	7 um
Base layer thickness	65 nm	45 nm

5.11 CONCLUSION

The influence of various design choices relating to the device geometry and doping of a HBT on its linearity, bandwidth and gain performance is investigated in this chapter. The results of the investigation are acquired through TCAD device simulations. The accuracy and reliability of the TCAD simulations are ensured by recreating published results of the reference HBT transistor, and validating TCAD simulation results of the reference HBT against the published measured results, as explained in more detail in Section 5.4. The results of these investigations can be used by designers to predict

how the linearity, bandwidth, current gain and the forward voltage gain of a HBT will be effected when the following device design parameters are varied: Collector doping, Spacer layer doping, Spacer layer thickness, Emitter width and Base thickness. The results offer a number of pointers and reveal a number of tradeoff options, which can be taken advantage of by designers depending on the desired linearity, bandwidth and gain performance of the HBT being designed, especially when intended to be used in analogue OEIC applications. Based on the results of the investigations, a series of modifications to the reference HBT are recommended in view of the goals in the project, which are presented in Section 5.10.

Chapter Six:

Conclusions and Future Work

6.1 CONCLUSIONS

This research has focused primarily on improving the linearity and Spurious-free Dynamic Range (SFDR) of the preamplifier within the photoreceiver in photonic links while retaining their high gain and bandwidth characteristics, in order to contribute to making them suitable for use in electronic warfare applications such as

radar warning receivers. The results that were achieved towards the goals as outlined in Section 1.3 will now be summarised.

In Chapters 2 and 3, the most suitable transistor technology, materials and amplifier topology for use in analogue OEIC's were determined through comparison between multiple alternatives in each category. Particularly, for the selection of the amplifier circuit topology, three popular transimpedance amplifier topologies were compared in terms of their performance in the various figures of merit of interest and from the findings of the comparison, the decision was reached that the distributed amplifier topology is best suited for the application type of interest as our investigations revealed it to be superior to the other two designs by far in terms of gain, gain-bandwidth product, and output 1dB compression point. The results of the investigations in Chapter 3 were presented at the Asia Pacific Microwave Conference 2009 partly sponsored by the IEEE Microwave Theory and Techniques Society and the IEEE Antennas and Propagation Society, and led to a publication titled "*A comparison of InP HBT transimpedance amplifier topologies for high dynamic range photonic links*" in the proceedings of the conference.

In Chapter 4, three different novel circuit design techniques for the improvement of the SFDR of HBT distributed amplifiers were developed and discussed in detail. Design examples of each of the techniques were demonstrated through simulation, the results of which were used to compare the performance of each of the techniques and their combinations with that of a published reference design in order to determine their performances and quantify the improvements achieved from each technique and each combination of techniques. Combinations of these techniques were also introduced and performance figures of design examples of the combinations were

determined through simulation, presented in a comparison table and discussed. The results were also used to determine the strengths and weaknesses of each of the techniques and each combination of the techniques, and based on the determined strengths and weaknesses, appropriate situations where each of the techniques or each of the combinations would be suitable for use were identified and discussed. The techniques developed and demonstrated in this chapter were reported in a research paper by the author which was peer reviewed and published under the title "*An investigation of tradeoff options for the improvement of spurious-free dynamic range in HBT transimpedance distributed amplifiers*" in the PIER L (Progress in Electromagnetic Research Letters) journal (http://www.jpier.org/PIER/) in 2012.

In Chapter 5, the influence of collector doping, spacer doping, spacer thickness, emitter width and base thickness on the gain, bandwidth and linearity of HBTs was investigated through simulations using commercial TCAD software and a significant contribution over previously known knowledge on the topic is made. The simulation model was validated against published results through DC I/V simulations. Also, where possible, the results of the investigation were validated against other published results. The findings from this investigation indicate a number of ways to improve the gain of an HBT transistor without any degradation of its linearity, as well as a number of other tradeoff options, which can be utilized towards the goal of improving the relevant figures of merit, listed in Section 1.3, of a HBT transistor and amplifier.

The results of the investigations on transistor geometry and doping from Chapter 5 can be combined with the developed circuit design techniques for SFDR improvement of transimpedance amplifiers from Chapter 4 to significantly overcome the limitations imposed by photoreceivers on potential use of optical links in analogue OEIC

applications. For example, the design techniques in Chapter 4 are shown to allow significant improvement of the Spurious-free Dynamic Range of HBT transimpedance distributed amplifiers, while the investigations in Chapter 5 reveal a number of ways to achieve higher HBT transistor gain without any degradation of HBT transistor linearity. Thus the knowledge contributed in these two chapters can be used in unison to attain HBT preamplifiers that are improved in terms of both gain and SFDR, and thus considerably more efficient for use in analogue OEIC applications.

6.2 FURTHER WORK

This work makes a notable contribution towards overcoming the limitations imposed on optical fibre links by the SFDR limitations of the preamplifier, with important indications, options and techniques relevant to overcoming this limitation having been developed, analysed and presented. Practical utilization of the techniques that were developed and the findings that were presented is considered to be the next logical step. Furthermore, the SFDR limitations of the preamplifier form only part of the obstacles in the way to the replacement of coaxial cables with optical fibre links in analogue applications as discussed in Section 1.2, which is the primary motivation behind this project. Some of the other major obstacles to achieving this larger goal are briefly discussed as follows:

1. SFDR limitation of the photodetector: Although the photodetector of the photoreceiver was briefly discussed in Chapter 2, this project mainly focused on the figures of merit of the transimpedance amplifier, i.e. the preamplifier of the

photoreceiver. While there have been some works that focus on the linearity of photodetectors [76, 77], works specifically focusing on improving the SFDR, along with retention of all the other relevant figures of merit, such as responsivity, bandwidth, etc. of the photoreceiver have been few and far between, especially the bandwidth, which is an important requirement in the target application type. As such, this problem needs to be addressed in further work.

2. SFDR limitation of the optical modulator: Despite past works focusing on the improvement of the SFDR of optical modulators and achieving an optical modulator SFDR value as high as 68 dB [15], the SFDR limitation of optical modulators remains the dominant obstacle towards achieving very high SFDR analogue optical links. Therefore further improvement of the SFDR of modulators should also be addressed in further work.

References

[1] A. Huber *et al.*, “Monolithic, high transimpedance gain (3.3K), 40 Gb/s InP–HBT photo receiver with differential outputs,” *Electron. Lett.*, vol. 35, pp. 897–898, 1999.

[2] Z. Lao *et al.*, “20-Gb/s 14-k transimpedance long-wavelength MSM-HEMT photo receiver OEIC,” *IEEE Photon. Technol. Lett.*, vol.10, pp. 710–712, 1998.

[3] P. Fay *et al.*, “High-speed digital and analog performance of low-noise integrated MSM-HEMT photoreceivers,” *IEEE Photon. Technol. Lett.*, vol. 9, pp. 991–993, 1997.

[4] P. Fay *et al.*, “Design, fabrication and performance of high speed monolithically integrated InGaAs/InAlAs/InP MSM/HEMT photoreceivers,” *J. Lightwave Technol.*, vol. 15, pp. 1871–1879, 1997.

[5] K. Yang *et al.*, “Design, modeling and characterization of monolithically integrated InP-Based (1.55 _m) high-speed (24 Gb/s) p-i-n/HBT front-end photoreceivers,” *J. Lightwave Technol.*, vol. 14, pp. 1831–1839, 1996.

[6] M. Yung, J. Jensen, R. Walden, M. Rodwell, G. Raghavan, K. Elliott, and W. Stanchina, “Highly integrated InP HBT optical receivers,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 219–227, Feb. 1999.

[7] H. D. Huber, R. Bauknecht, C. Bergamaschi, M. Bitter, A. Huber, T. Morf, A. Neiger, M. Rohner, I. Schnyder, V. Schwarz, and A. Jackel, “InP–InGaAs single HBT technology for photo receiver OEICs at 40 Gb/s and beyond,” *J. Lightwave Technol.*, vol. 18, pp. 992–1000, July 2000.

[8] D. Huber, M. Bitter, E. Gini, A. Neiger, T. Morf, C. Bergamaschi, and H. Jäckel, “50 GHz monolithically integrated InP/InGaAs PIN/HBTreceiver,” in *Proc. 11th Conf. Indium Phosphide and Related Mater.*, May 1999, pp. 6–7.

[9] K. Takahata, Y. Muramoto, H. Fukano, and Y. Matsuoka, “52 GHz bandwidth monolithically integrated WGPD/HEMT photo receiver with large O/E conversion factor of 105 V/W,” *Electron. Lett.*, vol. 35, no. 19, pp.1639–1640, Sept. 1999.

[10] Mekonnen, G.G.; Bach, H.-G.; Beling, A.; Kunkel, R.; Schmidt, D.; Schlaak, W., "80-Gb/s InP-based waveguide-integrated photoreceiver," *Selected Topics in Quantum Electronics, IEEE Journal of* , vol.11, no.2, pp. 356-360, March-April 2005.

[11] Cha, Jung-Ho; Kim, Jaeho; Kim, Choul-Young; Shin, Seong-Ho; Kwon, Young-Se, "Monolithic integration of InP-based HEMT and MSM photodiode using InGaAsP (λ=1.3μm) buffer", *Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers)*, vol. 44, no. 4B, pp. 2549-52, April 2005.

[12] Kraus, S.; Cohen-Elias, D.; Cohen, S.; Gavrilov, A.; Kami, O.; Swirski, Y.; Eisenstein, G.; Ritter, D., "High-Gain Top-Illuminated Optoelectronic Integrated Receiver," *Indium Phosphide & Related Materials, 2007. IPRM '07. IEEE 19th International Conference on* , vol., no., pp.77-80, 14-18 May 2007.

[13] Beling, A.; Bach, H.-G.; Kunkel, R.; Mekonnen, G.G.; Schmidt, D., "InP-based 1.55 μm high-speed photodetectors for 80 Gbit/s systems and beyond," *Transparent Optical Networks, 2005, Proceedings of 2005 7th International Conference* , vol.1, no., pp. 303-308 Vol. 1, 3-7 July 2005.

[14] Agilent ADS manuals, http://eesof.tm.agilent.com, copyright 2000-2005 © Agilent technologies.

[15] J. Scott, K. Ghorbani, A. Mitchell, M. Austin, and L. Bui, "Multi-wavelength variable drive-voltage modulator for use in high dynamic range photonic links," *Proceedings of Asia-Pacific Microwave Conference*, 2007.

[16] L. Boglione, "Power and linearity performance of a cascode In-GaP/GaAs HBT distributed amplifier for instrument applications," *2003 IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, 2217{2220, 2003.

[17] Koh, M. and G. Ellis, "Broadband linearization of InGaP/GaAs HBT power amplifier," *Proceedings of European Microwave Conference*, 878{881, Sep. 2010.

[18] Minghao, K., G. A. Ellis, and T. C. Soon, "Effects of output low impedance termination to linearity of GaAs HBT power amplifier," *2010 International Conference on Intelligent and Advanced Systems (ICIAS)*, 1-4, June 15-17, 2010.

[19] Ruan, Y., Y.-H. Liu, L. Chen, and Z.-S. Lai, "A 2.4 GHz fully-integrated SiGe BiCMOS power amplifier," *Journal of Electronics and Information Technology*, Vol. 33, No. 12, 3035-3039, Dec. 2011.

[20] Maazouzi, L. E., A. Mediavilla, and P. Colantonio, "A contribution to linearity improvement of a highly efficient Pa for WiMAX applications," *Progress In Electromagnetics Research*, Vol. 119, 59-84, 2011.

[21] Ciccognani, W., Limiti, E., Longhi, P. E., Mitrano, C., Nanni, A. and Peroni, M., "An ultra-broadband robust LNA for defence applications in AlGaN/GaN technology," IEEE IMS Dig., Anaheim, CA, May 2010.

[22] Pengelly, R., S. Sheppard, T. Smith, B. Pribble, S. Wood, and C. Platis, "Commercial GaN devices for switching and low-noise applications," CS MANTECH Conference, Palm Springs, CA, May 16-19, 2011.

[23] Lee, C.-I., W.-C. Lin, and J.-M. Lin, "Low-power and high-linearity SiGe HBT low-noise amplifier using IM3 cancellation technique," Microelectronic Engineering, Vol. 91, No. 3, 59-63, 2011.

[24] Pan, H.-Y. M. and L. E. Larson, "An improved broadband high linearity SiGe HBT differential amplifier," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 58, No. 8, 1685-1694, Aug. 2011.

[25] E. Cohen, Y. Betser, B. Sheinman, S. Cohen, S. Sidorov, A. Gavrilov, and D. Ritter, "75 GHz InP HBT Distributed Amplifier With Record Figures of Merit and Low Power Dissipation," *IEEE Trans. on Electron Devices*, vol. 53, 2006, pp. 2006-2008.

[26] B. Agarwal, A. E. Schmitz, J. J. Brown, M. Matloubian, M. G. Case, M. Le, M. Lui, and M. J. W. Rodwell, “112 GHz, 157 GHz, and 180 GHz InP HEMT traveling-wave amplifiers,” *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2553–2559, Dec. 1998.

[27] S. Chandrasekhar, L.M. Lunardi, A. H. Gnauck, R. A. Hamm, and G. J. Qua, “High-speed monolithic p-i-n/HBT and HPT/HBT photoreceivers implemented with simple phototransistor structure,” *IEEE Photon. Technol. Lett.*, vol. 5, pp. 1316–1318, Nov. 1993.

[28] Kobayashi, K.W.; Umemoto, D.K.; Block, T.R.; Oki, A.K.; Streit, D.C.; , "A monolithically integrated HEMT-HBT low noise high linearity variable gain amplifier," *Solid-State Circuits, IEEE Journal of* , vol.31, no.5, pp.714-718, May 1996.

[29] S.-S. Myoung; S.-H. Cheon; J.-G. Yook; , "Low noise and high linearity LNA based on InGaP/GaAs HBT for 5.3 GHz WLAN," *Gallium Arsenide and Other Semiconductor Application Symposium, 2005. EGAAS 2005. European* , vol., no., pp.89-92, 3-4 Oct. 2005.

[30] Kuebart, W.; Reemtsma, J.-H.; Kaiser, D.; Grosskopf, H.; Besca, F.; Luz, G.; Korber, W.; Gyuro, I.; , "High sensitivity InP-based monolithically integrated pin-HEMT receiver-OEIC's for 10 Gb/s," *IEEE Transactions on Microwave Theory and Techniques*, vol.43, no.9, pp.2334-2341, Sep 1995.

[31] J. Halamek, I. Viscor, and M. Kasal, "Dynamic range and acquisition system," *MEASUREMENT 2001*, Smolenice, Slovak Republic, 2001, pp. 45-47.

[32] M. Cooke, "Charting the Wireless Future (part 2)," *III-Vs Review*, vol. 19, pp. 23-27, 2006.

[33] W. Hafez, W. Snodgrass, M. Feng, "12.5 nm base pseudomorphic heterojunction bipolar transistors achieving fT=710 GHz and fMAX=340 GHz," *Applied Physics Letters*, vol.87, no.25, pp.252109-252109-3, Dec 2005.

[34] O. Esame, Y. Gurbuz, I. Tekin, A. Bozkurt, “Performance comparison of state-of-the-art heterojunction bipolar devices (HBTS) based on AlGaAs/GaAs, Si/SiGe and InGaAs/InP”, *Microelectronics Journal*, 35, p. 901-908, 2004.

[35] J. S. Rieh, et al., "SiGe HBTs with cutoff frequency of 350 Ghz," *2002 International Electron Devices Meeting Technical Digest*, San Fransisco, USA, December 8–11, 2002, pp. 771–774.

[36] M. Feng, W. Snodgrass, "InP Pseudormorphic Heterojunction Bipolar Transistor (PHBT) With Ft > 750GHz," *19th International Conference on Indium Phosphide & Related Materials*, 2007, pp.399-402, 14-18 May 2007.

[37] T. Ishibashi, H. Nakajima, H. Ito, S. Yamahata, and Y. Matsuoka, "Suppressed base-widening in AlGaAs/GaAs ballistic collection transistors", *Device Research Conf. Tech. Dig.*, 1990.

[38] T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, K. Mochizuki, T. Nakamura, "InGaP/GaAs HBT's with high-speed and low-current operation fabricated using WSi/Ti as the base

electrode and burying SiO2 in the extrinsic collector," *International Electron Devices Meeting, 1997. Technical Digest.*, pp.739-742, 7-10 Dec 1997.

[39] S. Voinigescu, P. Popescu, P. Banens, M. Copeland, G. Fortier, K. Howlett, M. Herod, D. Marchesan, J. Showell, S. Sziiagyi, H. Tran, J. Weng, "Circuits and technologies for highly integrated optical networking ICs at 10 Gb/s to 40 Gb/s," *IEEE Conference on Custom Integrated Circuits*, pp.331-338, 2001.

[40] L.M. Lunardi, "InP-based monolithically integrated photoreceivers," *International Conference on Indium Phosphide and Related Materials*, 1997, pp.471-474, 11-15 May 1997.

[41] S.-W. Seo, S.-Y. Cho, S. Huang, J. J. Shin; N. M. Jokerst, A. S. Brown, M. A. Brooke, "High-speed large-area inverted InGaAs thin-film metal-semiconductor-metal photodetectors," *IEEE Journal of Selected Topics in Quantum Electronics*, vol.10, no.4, pp. 686- 693, July-Aug. 2004.

[42] A. Beling, H.-G. Bach, R. Kunkel, G. G. Mekonnen, D. Schmidt, "InP-based 1.55 μm high-speed photodetectors for 80 Gbit/s systems and beyond," *Proceedings of Transparent Optical Networks, 7th International Conference, 2005*, vol.1, pp.303- 30, 3-7 July 2005.

[43] C.-C. Yang, Y.-H. Huang, T.-C. Peng, M.-C. Wu, C.-L. Ho, C.-C. Hong, I-M. Liu, Y.-T. Tsai, "Monte Carlo ray trace simulation for micro-ball-lens-integrated high-speed InGaAs p-i-n photodiodes," *Journal of Applied Physics*, vol. 101, no.3, pp.033107-033107-9, Feb 2007.

[44] J. G. Yang, S. Choi, Y. Jeong, K. Yang, "Theoretical and Experimental Study of the InP/InGaAs PIN Diode for Millimeter-wave MMIC Applications," *IEEE 19th International Conference on Indium Phosphide & Related Materials, 2007*, pp.133-136, 14-18 May 2007.

[45] T. Kim and K. Yang, "A New Large-Signal InP/InGaAs Single HBT Model Including Self-Heating and Impact Ionization Effects", *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 2141-2144, 2-7 June 2002.

[46] Y.T. Chieng and R.A. Minasian, *21st IREECON International*, Sydney, pp. 689-691, 14th–18th September 1987.

[47] T. Vanisri and C. Toumazou, "Low-Noise Optimisation of Current-Mode Transimpedance Optical Preamplifiers", *1993 IEEE International Symposium on Circuits and Systems*, pp. 966-969, 3-6 May 1993.

[48] T.T.Y. Wong, *Fundamentals of Distributed Amplification*, Artech House Inc., Norwood, MA, pp. 90, 1993.

[49] J. E. Green, R. C. Tozer, J. P. R. David, "Stability in Small Signal Common Base Amplifiers", *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 846 - 855 Volume: 60, Issue: 4, April 2013.

[50] K.W. Kobayashi, R. Esfandiari and A.K. Oki, "A Novel HBT Distributed Amplifier Design Topology based on Attenuation Compensation Techniques", *1994 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 447-450, 23-27 May 1994.

[51] B. Sewiolo, D. Kissinger, G. Fischer, and R. Weigel, "A high-gain high-linearity distributed amplifier for ultra-wideband-applications using a low cost SiGe BiCMOS technology," in *Wireless and Microwave Technology Conference, 2009. WAMICON'09. IEEE 10th Annual*, 2009.

[52] J. Walker, "Some observations on the design and performance of distributed amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 1, pp. 164–168, 1992.

[53] J. P. Fraysse, J. P. Viaud, P. Q. R. Campovecchio, M. Auxemery, R. Quere, "A 2 W, high efficiency, 2-8 GHz, cascode HBT MMIC power distributed amplifier," *2000 IEEE MTT-S Microwave Symposium Digest*, vol.1, pp.529-532, 2000.

[54] S. A. Maas, B. L. Nelson, and D. L. Tait, "Intermodulations in HBTs," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 442–448, Mar. 1992.

[55] A. Samelis and D. Pavlidis, "Mechanisms determining third order intermodulation distortion in AlGaAs/GaAs HBTs," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2374–2380, Dec. 1992.

[56] J. Lee, W. Kim, T. Rho, and B. Kim, "Intermodulation mechanism and linearization of AlGaAs/GaAs HBT's," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2065–2072, Dec. 1997.

[57] N. L. Wang, W. J. Ho, and J. A. Higgins, "AlGaAs/GaAs HBT linearity characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1845–1850, Oct. 1994.

[58] K. W. Kobayashi, J. C. Cowles, L. T. Tran, A. Gutierrez-Aitken, M. Nishimoto, J. H. Elliott, T. R. Block, A. K. Oki, and D. C. Streit, "A 44-GHz-high IP3 InP HBT MMIC amplifier for low DC power millimeter-wave receiver applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1188–1194, Sept. 1999.

[59] N. L. Wang, W. J. Ho, and J. A. Higgins, "AlGaAs/GaAs HBT linearity characteristics," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1845–1850, Oct. 1994.

[60] P. Asbeck, "HBT linearity and basic linearization approaches," presented at the *IEEE MTT-S Int. Microwave Symp.Workshop*, Baltimore, MD, June 1998.

[61] M. Iwamoto, T. S. Low, C. P. Hutchinson, J. B. Scott, A. Cognata, X. Qin, L. H. Camnitz, P. M. Asbeck, and D. C. D'Avanzo, "Influence of collector design on InGaP/GaAs HBT linearity," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, Jun. 2000, pp. 757–760.

[62] K. W. Kobayashi, A. K. Oki, J. Cowles, L. T. Tran, P. C. Grossman, T. R. Block, D. C. Streit, "The voltage-dependent IP3 performance of a 35-GHz InAlAs/InGaAs-InP HBT amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 3, pp. 66-68, March 1997.

[63] J. Lee, W. Kim, Y. Kim, T. Rho, B. Kim, "Intermodulation mechanism and linearization of AlGaAs/GaAs HBTs," *IEEE Trans. on Microwave Theory Tech.*, vol. 45, no. 12, pp. 2065-2072, Dec. 1997.

[64] W. Kim, S. Kang, K. Lee, M. Chung, Y. Yang, B. Kim, “The effects of Cbc on the linearity of AlGaAs/GaAs power HBTs,” *IEEE Trans. on Microwave Theory Tech.*, vol. 49, no. 7, pp. 1270-1276, Jul. 2001.

[65] C.-M. Wang, H.-T. Hsu, H. C. Shu, Y.-M. Hsin, “High linearity InGaP/GaAs power HBTs by collector design,” *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 58- 60, Feb. 2004.

[66] M.-C. Tu, H.-Y. Ueng, Y.-C. Wang, “Performance of High-Reliability and High-Linearity InGaP/GaAs HBT PAs for Wireless Communication,” *IEEE Trans. on Electron Devices*, vol. 57, no. 1, pp.188-194, Jan. 2010.

[67] T. Tauqeer, J. Sexton, F. Amir, M. Missous, “Two-Dimensional Physical and Numerical Modelling of InP-based Heterojunction Bipolar Transistors,” *International Conference on Advanced Semiconductor Devices and Microsystems*, 2008, pp.271-274, 12-16 Oct. 2008.

[68] H. Kaatuzian, E. Javadi, S. Khatami, “The Effects of Structural Parameters Alteration on Improvement of Current Gain and High Frequency Performance of a AlGaAs/GaAs SHBT, ” *2012 Symposium on Photonics and Optoelectronics (SOPO)*, pp.1-4, 21-23 May 2012.

[69] Silvaco TCAD from Silvaco Data Systems, Inc. [Online]. Available: www.silvaco.com.

[70] D. M. Caughey, R. E. Thomas, “Carrier mobilities in silicon empirically related to doping and field,” *Proceedings of the IEEE*, vol. 55, pp. 2192-2193, 1967.

[71] W. Shockley, W. T. Read, “Statistics of the Recombination of Holes and Electrons,” *Phys. Rev. 87*, pp. 835-842, 1952.

[72] R. N. Hall, “Electron Hole Recombination in Germanium,” *Phys. Rev. 87*, pp. 387, 1952.

[73] J. Dziewior, W. Schmid, “Auger Coefficient for Highly Doped and Highly Excited Silicon,” *Appl. Phys. Lett.*, Vol. 31, pp. 346-348, 1977.

[74] S. Selberherr, “Analysis and Simulation of Semiconductor Devices,” Wien, New York: *Springer-Verlag*, 1984.

[75] A. G. Chynoweth, “Ionisation Rates for Electrons and Holes in Silicon,” *Phys. Rev. 109*, pp. 1537-1540, 1958.

[76] K. J. Williams, L. T. Nichols, R. D. Esman, “Photodetector nonlinearity limitations on a high-dynamic range 3 GHz fiber optic link,” *Journal of Lightwave Technology*, vol.16, no.2, pp. 192-199, Feb 1998.

[77] A. Beling, Z. Li, Y. Fu, H. Pan, J. C. Campbell, “High-power and high-linearity photodiodes,” *2011 IEEE Photonics Conference (PHO)*, vol., no., pp.19,20, 9-13 Oct. 2011.

[78] S.-E. Hamran, "Radar Performance of Ultra Wideband Waveforms", *Radar Technology*, Guy Kouemou (Ed.), ISBN: 978-953-307-029-2, InTech, 2010, Available from: "http://www.intechopen.com/books/radar-technology/radar-performance-of-ultra-wideband-wave-forms".

[79] B. Masella, B. Hraimel, X. Zhang, “Enhanced Spurious-Free Dynamic Range Using Mixed Polarization in Optical Single Sideband Mach–Zehnder Modulator,” *Journal of Lightwave Technology*, vol. 27, no. 15, pp. 3034-3041, 01 Aug. 2009.

[80] S. Miura, O. Wada, H. Hamaguchi, M. Ito, M. Makiuchi, K. Nakai, T. Sakurai, "A monolithically integrated AlGaAs/GaAs p-i-n/FET Photoreceiver by MOCVD," *IEEE Electron Device Letters*, vol.4, no.10, pp.375,376, Oct 1983.

[81] M. Ito, O. Wada, K.. Nakai, T. Sakurai, "Monolithic integration of a metal-semiconductor-metal photodiode and a GaAs preamplifier," *IEEE Electron Device Letters*, vol.5, no.12, pp.531,532, Dec 1984.

[82] K. D. Pedrotti, R. L. Pierson, R. B. Nubling, C. W. Farley, E. A. Sovero, M. F. Chang, "Ultra-High-Speed Pin/hbt Monolithic Oeic Photoreceiver," *49th Annual Device Research Conference*, 1991, vol., no., pp.VA_2,0_65, 17-19 June 1991.

[83] J.-S. Rieh, D. Klotzkin, O. Qasaimeh, L.-H. Lu, K. Yang, L. P. B. Katehi, P. Bhattacharya, E. T. Croke, "Monolithically integrated SiGe-Si PIN-HBT front-end photoreceivers," *IEEE Photonics Technology Letters*, vol.10, no.3, pp.415,417, March 1998.

[84] Y. Zhang, C. S. Whelan, R. Leoni, P. F. Marsh, W. E. Hoke, J. B. Hunt, C. M. Laighton, T. E. Kazior, "40-Gbit/s OEIC on GaAs substrate through metamorphic buffer technology," *IEEE Electron Device Letters*, vol.24, no.9, pp.529,531, Sept. 2003.

[85] G. G. Mekonnen, H.-G. Bach, A. Beling, R. Kunkel, D. Schmidt, W. Schlaak, "80-Gb/s InP-based waveguide-integrated photoreceiver," *IEEE Journal of Selected Topics in Quantum Electronics*, vol.11, no.2, pp.356,360, March-April 2005.

[86] M. I. Skolnik, "An introduction to radar", *Radar Handbook*, 2nd Edition, McGraw-Hill, 1990, Chapter 1, pp. 1.14-1.18.

[87] M. Abe, T. Mimura, N. Yokoyama, H. Ishikawa, "New technology towards GaAs LSI/VLSI for computer applications," *IEEE Transactions on Electron Devices*, vol.29, no.7, pp.1088-1094, Jul 1982.

[88] P. M. Asbeck, M.-C. F. Chang, J. A. Higgins, N.-H. Sheng, G. J. Sullivan, K.-C. Wang, "GaAlAs/GaAs heterojunction bipolar transistors: issues and prospects for application," *IEEE Transactions on Electron Devices*, vol.36, no.10, pp.2032,2042, Oct 1989.

[89] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proceedings of the IEEE*, vol.70, no.1, pp.13,25, Jan. 1982.

[90] S. M. Sze, Kwok K. Ng, “JFETs, MESFETs and MODFETs”, *Physics of Semiconductor Devices*, 3rd edition, John Wiley & Sons Inc., 2007, Chapter 7, Section 7.3, pp. 401-410.

[91] R. Ludwig, P. Bretchko, "Active RF Components", *RF Circuit Design: Theory and Applications*, Prentice-Hall Inc., 2000, Chapter 6, Sections 6.3.1 and 6.5, pp 312-314, 338-341.

[92] S. M. Sze, "Bipolar Transistor and Related Devices", *Semiconductor Devices: Physics and Technology*, 2nd edition, John Wiley & Sons Inc., 2002, Chapter 5, Section 5.4, pp. 151-155.

[93] D. Decoster, J. Harari, "Phototransistors", *Optoelectronic Sensors*, John Wiley & Sons Inc., 2009, Chapter 4, Section 4.2.1, pp. 112-113.

[94] S. M. Rezaul Hasan, "A 5GHz CMOS voltage-current feedback wide-band transimpedance amplifier for optical transceivers", *10th IEEE International Conference on Electronics, Circuits and Systems*, 2003, Vol. 2, pp. 567 - 570.

[95] J. B. Beyer, S. N. Prasad, R. C. Becker, J. E. Nordman, G. K. Hohenwarter, "MESFET Distributed Amplifier Design Guidelines", *IEEE Transactions on Microwave Theory and Techniques*, vol.32, no.3, March 1984.

[96] F. Reif, *Fundamentals of Statistical and Thermal Physics*, 1st edition, McGraw Hill, 1965, pp. 341.

[97] Z. Shouli, X. Deping, Q. Yali, "Considerations of dopant-dependent bandgap narrowing for accurate device simulation in abrupt HBTs", *Journal of Semiconductors*, vol. 30, no. 4, April 2009.

[98] T. Gonzalez Sanchez, J. E. Velazquez Perez, P. M. Gutierrez Conde, D. Pardo Collantes, "Electron transport in InP under high electric field conditions", *Semiconductor Science and Technology*, vol. 7, pp. 31-6,1992.

[99] V. Balynas, A. Krotkus, A. Stalnionis, A. T. Gorelionok, N. M. Shmidt, and J. A. Tellefsen, "Time-resolved, hot-electron conductivity measurement using an electro-optic sampling technique, " *Applied Physics A (Solids and Surfaces)*, vol. 51, issue 4, pp. 357-360, October 1990.

[100] S. Datta, K. P. Roenker, M. M. Cahay, W. E. Stanchina, "Implications of hole vs. electron transport properties for high speed Pnp heterojunction bipolar transistors," *Solid State Electronics*, vol. 43, pp. 73-79, 1999.

[101] J. W. Parks, A. W. Smith, K. F. Brennan, L. E. Tarof, "Theoretical study of device sensitivity and gain saturation of separate absorption, grading, charge, and multiplication InP/InGaAs avalanche photodiodes, " *IEEE Transactions on Electron Devices*, vol. 43, no. 12, pp. 2113-2121, December 1996.

[102] M. F. Chang, *Current Trends in Heterojunction Bipolar Transistors*, World Scientific Publishing Co. Pte. Ltd., pp. 406, 1996.

[103] H. Veenstra, J. R. Long, *Circuit and Interconnect Design for RF and High Bit-rate Applications*, Spinger, 2008, pp. 91.

[104] D. C. Vacanti, "Microwave and millimeterwave radar sensors," U.S. Patent 7737880, July 15, 2010.

[105] J. Shah, "DARPA'S EPIC program: electronic and photonic integrated circuits on Si," *2nd IEEE International Conference on Group IV Photonics, 2005*, pp. 1-3, 21-23 Sept. 2005.

[106] S. Taher and J. Scott, "A comparison of InP HBT transimpedance amplifier topologies for high dynamic range photonic links," *Proceedings of Asia-Pacific Microwave Conference*, 2009.

[107] S. Taher and J. Scott, "An investigation of tradeoff options for the improvement of spurious-free dynamic range in HBT transimpedance distributed amplifiers," *Progress In Electromagnetics Research Letters*, Vol. 30, pp. 67-79, 2012.

[108] J. M. Rollett, "Stability and Power-Gain Invariants of Linear Twoports," *IRE Transactions on Circuit Theory*, vol.9, no.1, pp. 29-32, Mar 1962.

[109] K. W. Kobayashi, "An InP HBT common-base amplifier with tunable transimpedance for 40 Gb/s applications," *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2002. 24th Annual Technical Digest*, pp. 155-158, 20-23 Oct. 2002.

[110] J. Rue, M. Itzler, N. Agrawal, S. Bay, W. Sherry, "High performance 10 Gb/s PIN and APD optical receivers," *Proceedings of 49th Electronic Components and Technology Conference, 1999*, pp. 207-215, 1999.

[111] M. Iwamoto, P. M. Asbeck, T. S. Low, C. P. Hutchinson, J. B. Scott, A. Cognata, X. Qin, L. H. Camnitz, D. C. D'Avanzo, "Linearity characteristics of GaAs HBTs and the influence of collector design," *IEEE Transactions on Microwave Theory and Techniques*, vol.48, no.12, pp. 2377-2388, Dec 2000.

[112] D. Ritter, R. A. Hamm, A. Feygenson, M. B. Panish, S. Chandrasekhar, "Diffusive base transport in narrow base InP/$Ga_{0.47}In_{0.53}As$ heterojunction bipolar transistors", *Applied Physics Letters*, vol.59, pp. 3431-3433, 1991.

[113] S. M. Sze, *High Speed Semiconductor Devices*, Wiley, 1990, pp. 335.